AIONYX

Datasheet

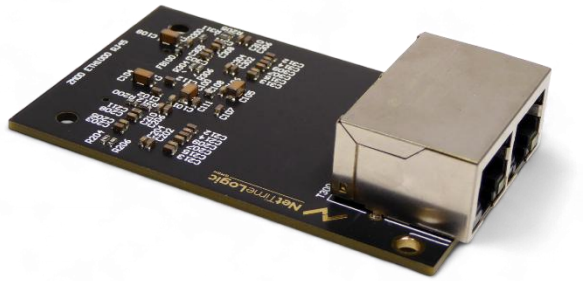
ZmEth1000RJ45

This Zmod™ compatible module features two RJ45 connectors supporting 10/100/1000 Mbit Ethernet, powered by two TI DP83869HM High Immunity Ethernet PHYs connected via two separate RGMII interfaces. Offering minimal jitter, low latency, and SyncE support, this module is ideal for industrial, power and utilities, telecom and real-time applications.

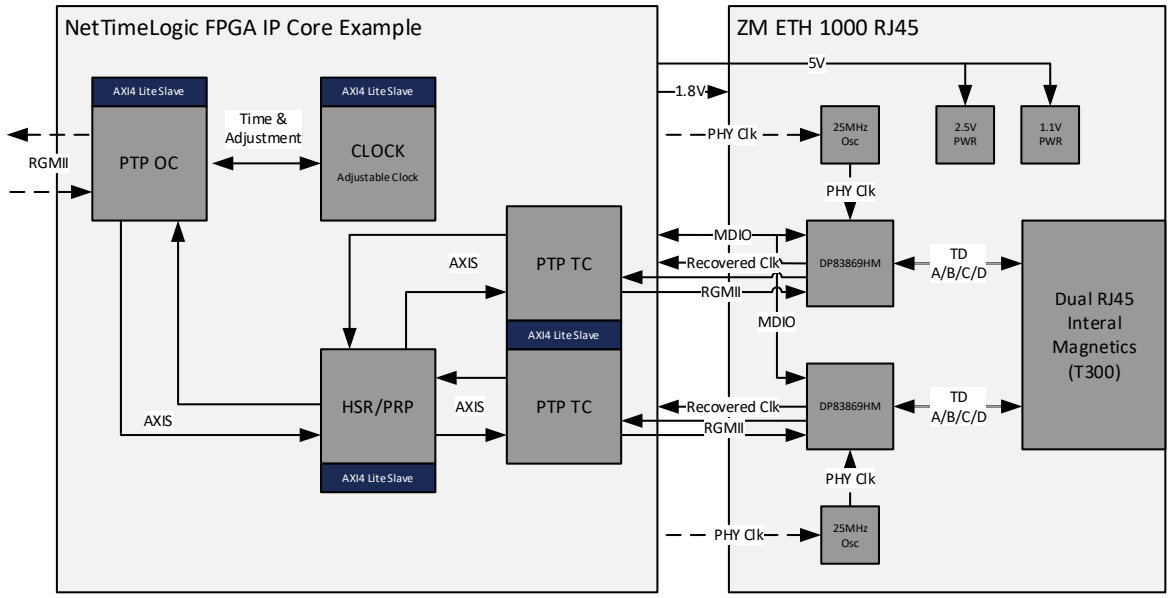
Key Features:

- Two 10/100/1000 Mbit/s RJ45 Ethernet Ports
- MDIO Interface to the PHYs
- SyncE (Synchronous Ethernet) Support on Both Ports
- RGMII Interface to FPGA
- Ultra-Low Latency (< 384 ns for 1000Base-T)

Module:



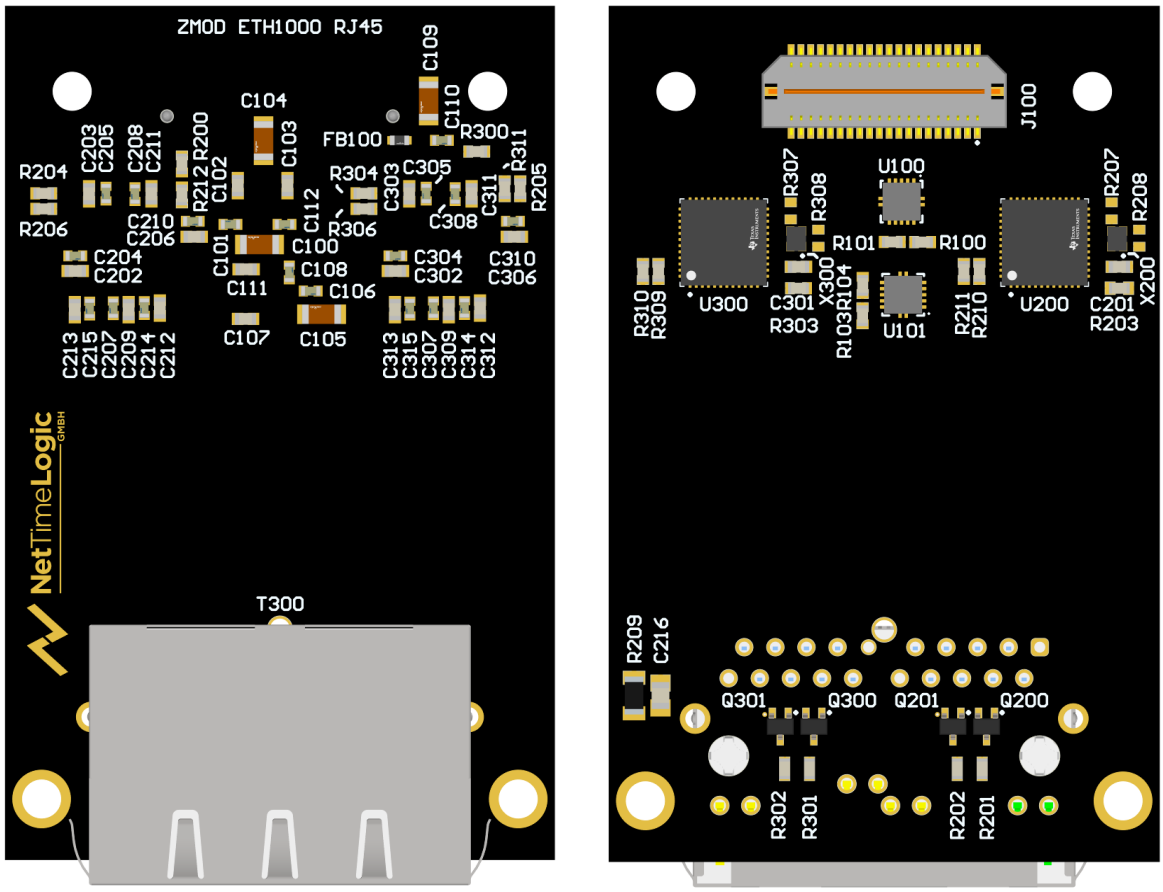
Block Diagram:



Specification:

Ethernet PHY	2x TI DP83869HM
PHY Interface	2x RGMII
PHY CLK	2x onboard 25MHz Oscillator Assembly of 0 Ohm resistors (R207/R307 and R208/R308) allows providing the clock from the FPGA 2x PHY programable Output clock
Status LEDs	Link and Traffic LEDs (LED_0/Green & LED_2/Yellow)
Configuration PHY	Shared MDIO Interface (PHY A Addr: 0x03; PHY B Addr: 0x0C)
Power	5V and 1.8V provided via the connector 2.5V and 1.1V generated onboard for the two PHYs Total Power Consumption ~1.7W for RGMII 1G
Base Connector	Samtec QSE-020-01-F-D-A

Module Overview & Pin Description:



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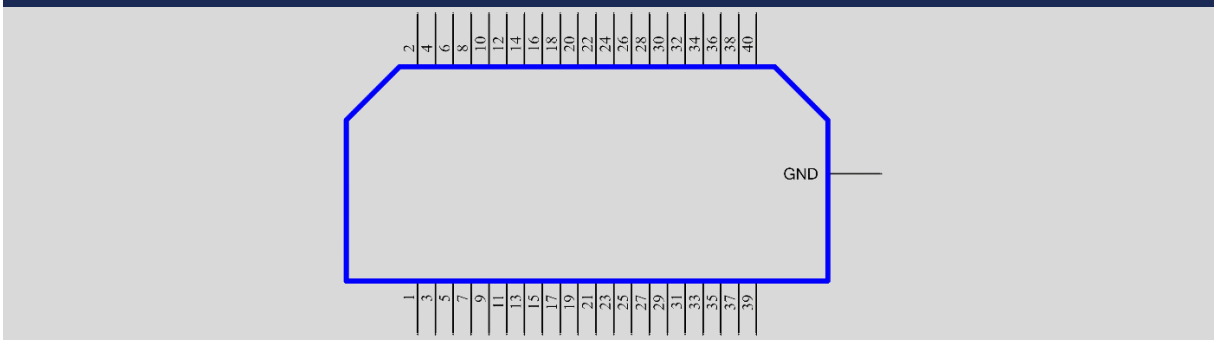
J100 (QTE-020 SYZYGY standard connector)



Pin	Signal	I/O	Description	Pin	Signal	I/O	Description
1	SCL	I/O	Unused on this module	2	5V	I	5V DC supply for the module
3	SDA	I/O	Unused on this module	4	R_GA	-	Unused on this module
5	RGMII RX CLK (PHY A)	O	Receive Clock in RGMII Mode (Clock Pin on FPGA)	6	RGMII TX CLK (PHY A)	I	Transmit Clock in RGMII Mode
7	RGMII RX D0 (PHY A)	O	Receive Data Bit 0 in RGMII Mode	8	RGMII TX D0 (PHY A)	I	Transmit Data Bit 0 in RGMII Mode
9	RGMII RX D1 (PHY A)	O	Receive Data Bit 1 in RGMII Mode	10	RGMII TX D1 (PHY A)	I	Transmit Data Bit 1 in RGMII Mode
11	RGMII RX D2 (PHY A)	O	Receive Data Bit 2in RGMII Mode	12	RGMII TX D2 (PHY A)	I	Transmit Data Bit 2 in RGMII Mode
13	RGMII RX D3 (PHY A)	O	Receive Data Bit 3 in RGMII Mode	14	RGMII TX D3 (PHY A)	I	Transmit Data Bit 3 in RGMII Mode
15	Clock Output (PHY A)	O	25 MHz Clock Output from PHY A (Clock Pin on FPGA)	16	PHY CLK (PHY A)	I	Default unused (on board oscillator X200)
17	RGMII RX CTL (PHY A)	O	Receive Control in RGMII	18	RGMII TX CTL (PHY A)	I	Transmit Control in RGMII
19	PHY CLK (PHY B)	I	Default unused (on board oscillator X300)	20	RGMII RX CLK (PHY B)	O	Receive Clock in RGMII Mode (Clock Pin on FPGA)
21	RGMII TX D3 (PHY B)	I	Transmit Data Bit 3 in RGMII Mode	22	Clock Output (PHY B)	O	25 MHz Clock Output from PHY B (Clock Pin on FPGA)
23	RGMII TX D2 (PHY B)	I	Transmit Data Bit 2 in RGMII Mode	24	Reset N (PHY A)	I	Active Low PHY Reset
25	RGMII TX D1 (PHY B)	I	Transmit Data Bit 1 in RGMII Mode	26	RGMII RX D3 (PHY B)	O	Receive Data Bit 3 in RGMII Mode
27	RGMII TX D0 (PHY B)	I	Transmit Data Bit 0 in RGMII Mode	28	RGMII RX D2 (PHY B)	O	Receive Data Bit 2in RGMII Mode
29	RGMII TX CLK (PHY B)	I	Transmit Clock in RGMII Mode	30	RGMII RX D1 (PHY B)	O	Receive Data Bit 1 in RGMII Mode
31	SMI MDC	I	Management Clock	32	RGMII RX D0 (PHY B)	O	Receive Data Bit 0 in RGMII Mode
33	SMI MDIO	I/O	Management Data I/O	34	RGMII RX CTL (PHY B)	O	Receive Control in RGMII
35	RGMII TX CTL (PHY B)	I	Transmit Control in RGMII	36	Reset N (PHY B)	I	Active Low PHY Reset
37	RSVD	-	Reserved	38	RSVD	-	Reserved
39	1V8	I	1.8V DC supply for the module	40	3V3	I	Unused on this module

Note: The module uses the SYZYGY standard connector and follows the same form factor. The module is not fully compliant with the SYZYGY standard but remains electrically compatible.

Dual RJ45			
T300	2x RJ45	In/Out	10/100/1000 Mbit Ethernet Connector with integrated magnetics

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