UniversalNetRed

The Universal Net Red solution is a combination of network redundancy and PTP time synchronization cores provided by NetTimeLogic. It can be tailored to specific needs by adding and removing individual cores. It can be used as network redundancy co-processor with or without time synchronization awareness. Therefore it is especially suited where high availability and synchronization is required. Synchronization can be provided either only on the HSR forwarding path or also used by a PTP OC

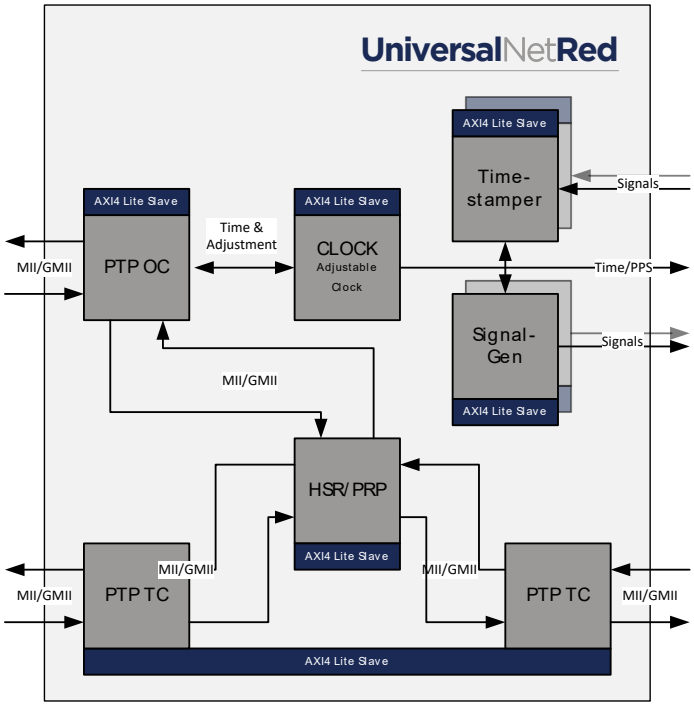
Key Features:

- HSR and PRP support
- PTP OC and TC using the adjustable clock
- Signal time stampers and signal generators
- 100% hardware only solution
- Vendor independent

Typical Applications:

- Ethernet based automation networks
- High availability environments
- Substation automation
- Distributed data acquisition
- Test and measurement
- Legacy component integration

IP Core Architecture:



Specification:

Cores	Parallel Redundancy Protocol (PRP) and High Availability Seamless Redundancy (HSR) with optional ModeX support RedBox support for up to 256 Nodes PTP Ordinary and Transparent Clock cores with Layer 2 and Ipv4, P2P delay mechanism, 1 step support Adjustable Counter Clock with PI servos Signal Timestamper and Signal Generator aligned with clock
Performance	Offloading synchronization and network redundancy Full line speed frame processing 10/100/1000 Mbit/s support, intercepts (R)(G)MII interfaces between MAC and PHY (no MAC required)
Portability	100% hardware only solution, no dependency on external CPU Vendor independent, written in plain VHDL Low footprint and low frequency requirements
Accuracy	Sub microsecond synchronization With 50ppm Oscillator: +/- 100ns (for OC and PPS)
Modularity	Modular system; synchronization cores can be added or removed depending on the needs
Configuration	No CPU required, standalone configuration with signals Axi4 lite slave support, for status and configuration

Deliverables:

- Ip core in plain VHDL
- Testbench in plain VHDL
- Reference Design
  - Top level VHDL file
  - Timing Constraint SDC files
  - Vivado/Quartus Project file

Related Products:

- HSR & PRP Core
- PTP Ordinary Clock
- PTP Transparent Clock
- PTP Hybrid Clock
- Universal Time Sync
- Adjustable Clock
- Signal Timestamper
- Signal Generator

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