

# TodSlaveClock

A low-footprint, highly configurable, 100% hardware only NMEA/UBX/TSIP Time of Day (ToD) Slave Clock solution, specifically designed for high-performance distributed systems. Allows standalone synchronization via NMEA/UBX/TSIP messages from a NMEA/UBX/TSIP source e.g. GPS receivers via UART. All frame parsing and calculations are done completely in hardware.

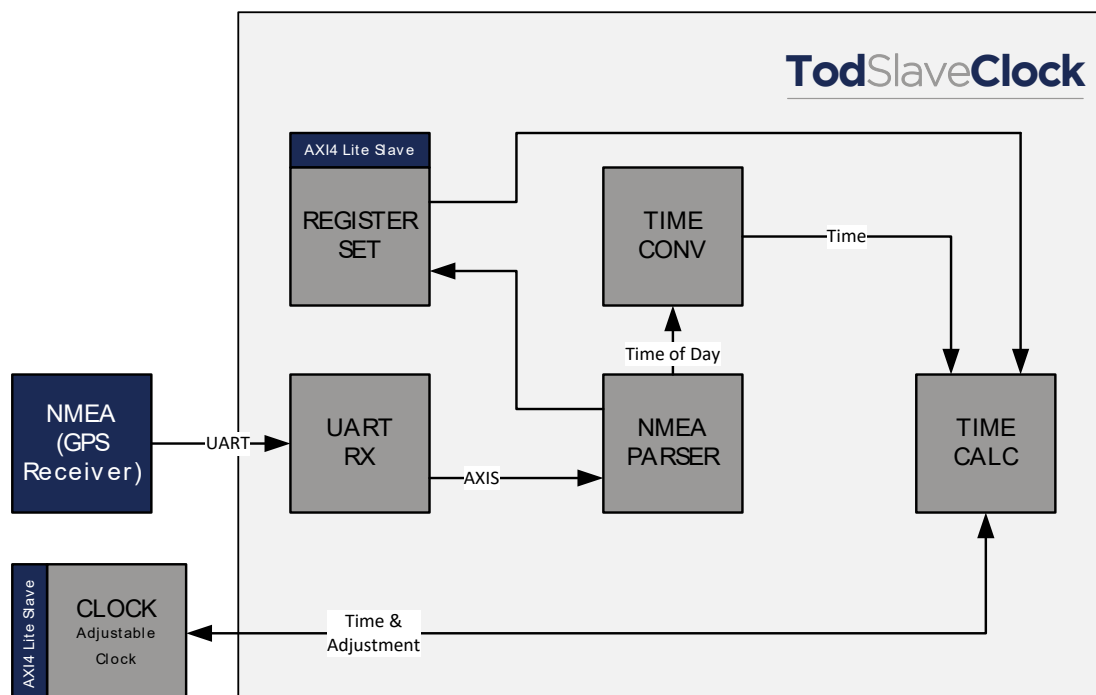
## Key Features:

- NMEA/UBX/TSIP/ESIP (ToD) Slave Clock
- 100% hardware only solution
- Vendor independent
- Hardware frame parser
- Time, UTC, Spoofing, Jamming, Satellite Status Support
- Hardware time conversion
- Quality supervision

## Typical Applications:

- Legacy Networks
- Time converters
- Time servers with GNSS
- Substation automation
- Distributed data acquisition
- Test and measurement
- Etc.

## IP Core Architecture:



## Specification:

NMEA	<p>Supports NMEA GxZDA, GxRMC, GxGSA, GxGSV, GxGGA and GxUTC messages</p> <p>Supports UBX NAV_TIME_UTC, NAV_TIME_LS, NAV_STATUS, MON_HW and NAV_SAT messages</p> <p>Supports TSIP TIMING_INFO, POSITION_INFO, RECEIVER_STATUS, SYSTEM_ALARMS and SAT_INFO messages</p> <p>Supports ESIP CRW, CRY, CRJ messages</p> <p>UTC handling and Status information for UBX/TSIP/ESIP</p> <p>Hardware UART with configurable baud rate: 9.6k - 1m baud</p> <p>Hardware conversion from time of day format to seconds since midnight 1.1.1970 including leap years.</p> <p>Hard time set to the parsed second plus configurable offset at the second overflow of the local clock.</p>
Performance	Offload parsing, time format conversion and synchronization.
Portability	<p>100% hardware only solution, no dependency on external CPU or UART</p> <p>Vendor independent, written in plain VHDL</p> <p>Low footprint and low frequency requirements</p>
Modularity	Slim and standardized interfaces are used
Configuration	<p>No CPU required, standalone configuration with signals</p> <p>Axi4 lite slave support, for status and configuration</p>

## Deliverables:

- Ip core in plain VHDL
- Testbench in plain VHDL
- Reference Design with 1 PPS input and output
  - Top level VHDL file
  - Timing Constraint SDC files
  - Vivado/Quartus Project file

## Related Products:

- PPS Master/Slave
- PTP Ordinary Clock
- PTP Grandmaster Clock
- PTP Hybrid Clock
- IRIG Master/Slave
- Adjustable Clock
- Signal Timestamper
- Signal Generator



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