

Capabilities and benefits

## **Time Card with PCIe PTM support**

- What is PCIe PTM?
- How to get PCIe PTM on the Time Card
- Requirements, Capabilities and Benefits
- Measurements
- Conclusion
- Future Work and Vision

# What is PCIe PTM?

Precision Time Measurement (PTM)

- **Introduced in PCI-SIG<sup>®</sup> PCI Express 3.0 specification**
  - Released in 2010
- **Aligns PCIe devices to a common clock source for highly accurate timing**
  - Protocol of timing measurement and synchronization messages
- **Nanosecond-Level Accuracy: Ensures precise coordination across devices, minimizing clock drift**
- **More information: a very good and detailed presentation:**
  - [Precision Time Within the Computer - In the Last Centimeters \(Kevin B. Stanton\)](#)

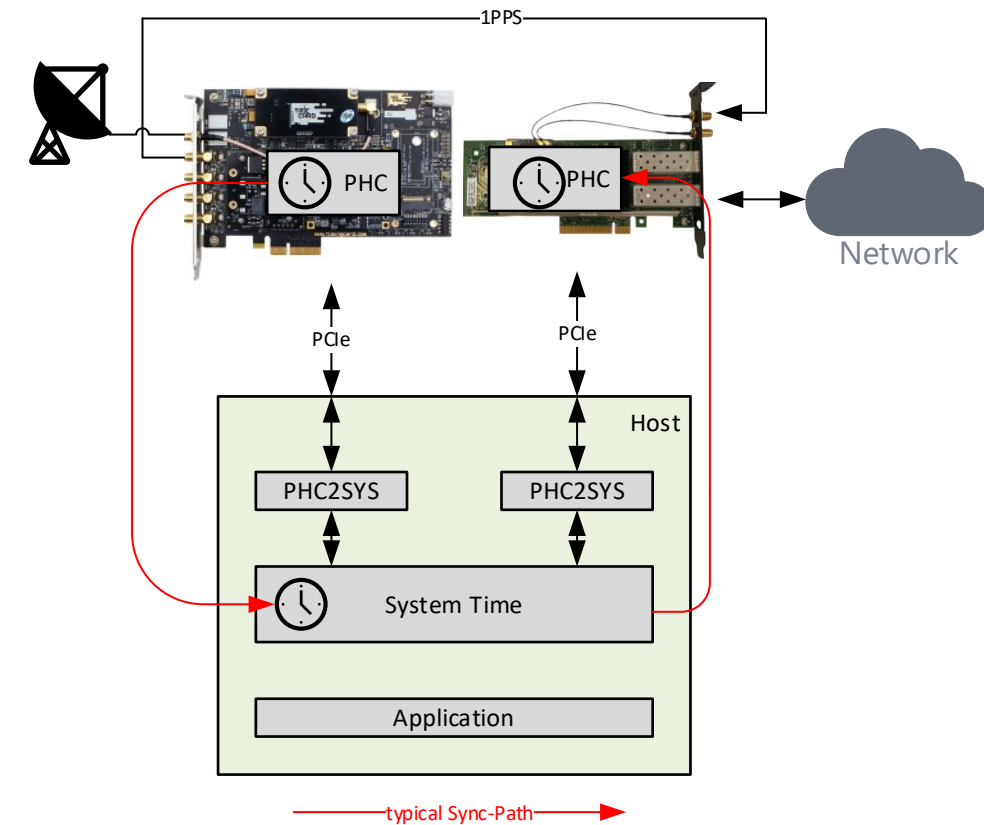


# What is PCIe PTM?

How does it work without PTM

- **Time Card without PTM:**

- Delay between reading the PHC value and updating the System Time is load dependent
- 1PPS over an external wire to the NIC is used to achieve the required accuracy



# What is PCIe PTM?

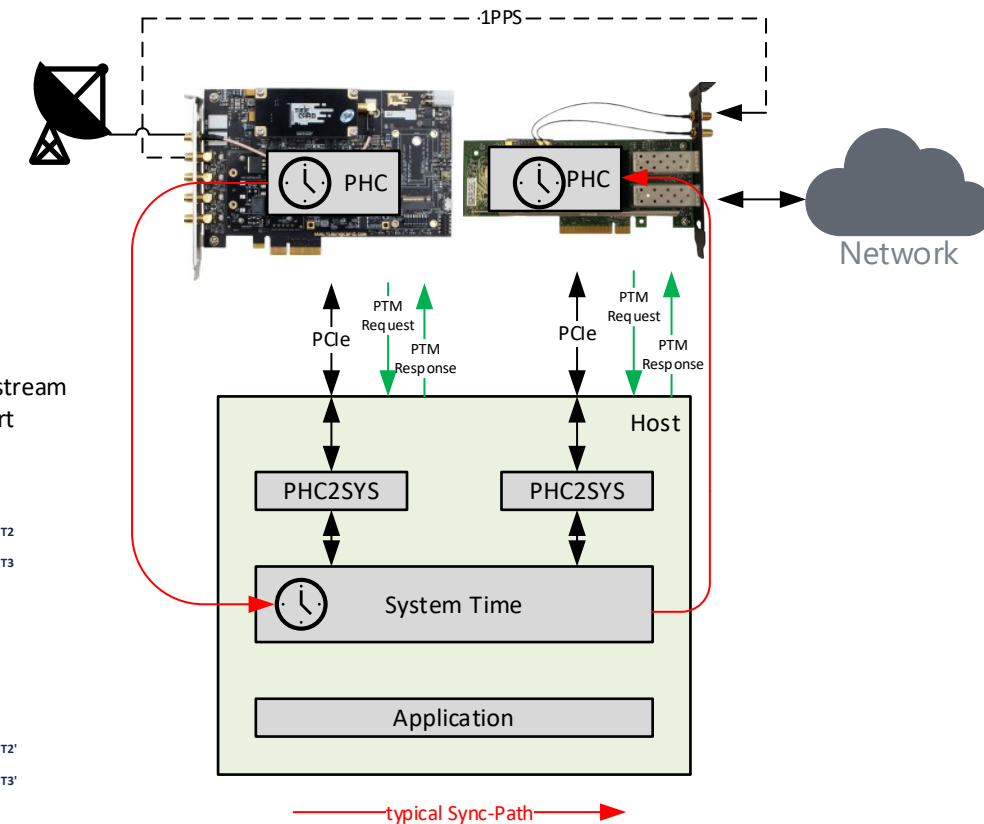
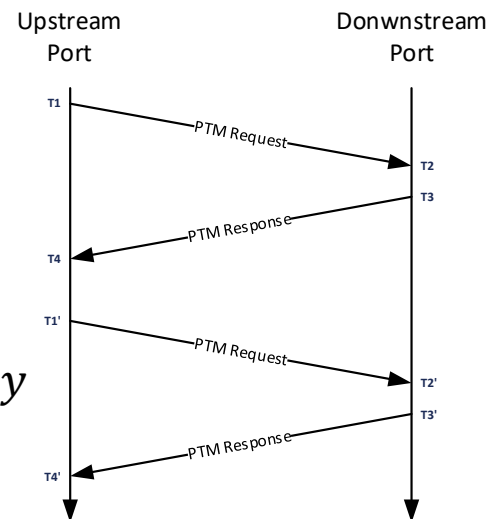
How does it work with PTM

- **Time Card with PTM:**

- Time Card sends PTM Requests
- Host responds with PTM Responses
- LinkDelay can be calculated
- Time can be calculated

$$LinkDelay = \frac{((t4 - t1) - (t3 - t2))}{2}$$

$$PTM \text{ Master Time @ } t1' = t2' - LinkDelay$$



# How to get PCIe PTM on the Time Card?

Starting point

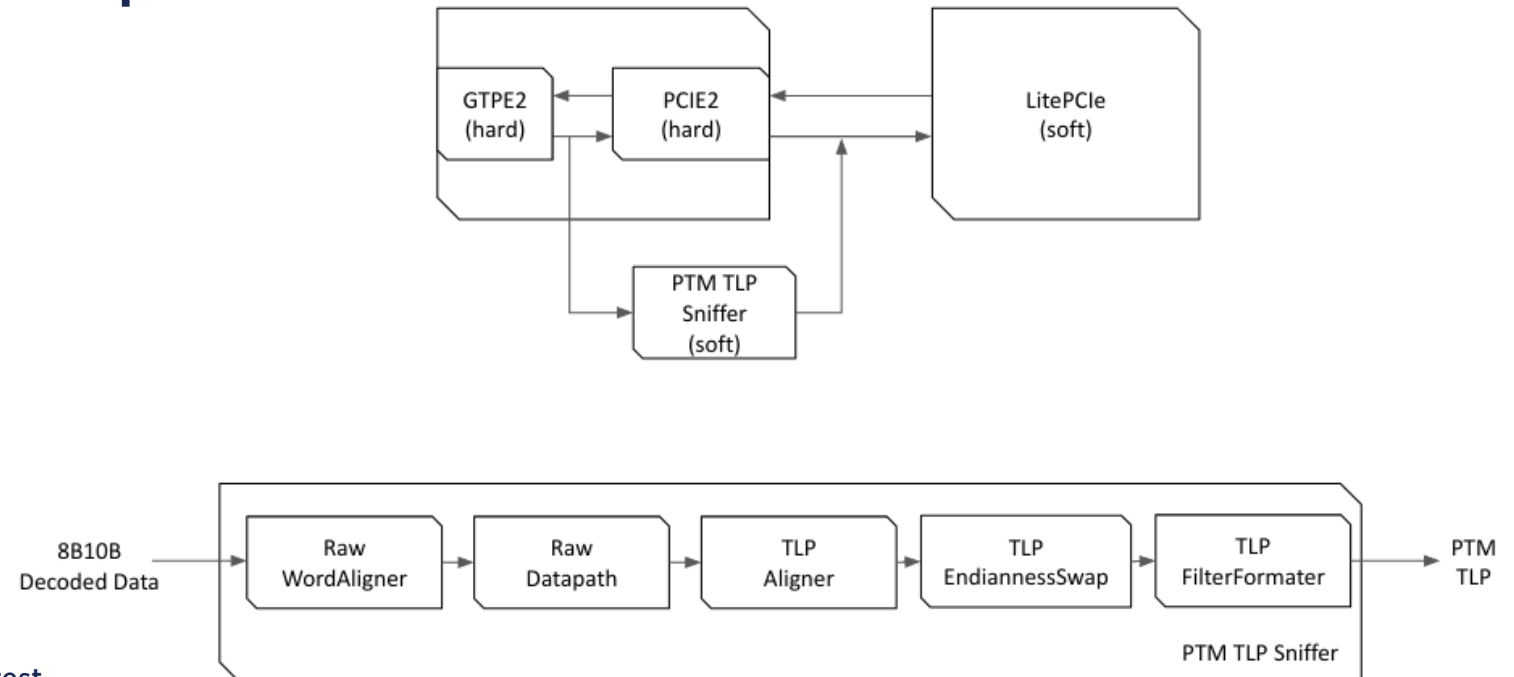
- **AMD AXI Memory Mapped to PCI Express (PCIe) Gen2 bridge**  
→ no PTM support
- **Initial LitePCIe version (open-source)**  
→ no PTM support
- **LitePCIe with PTM support**  
→ finally PTM support on an AMD FPGA 😊  
[https://github.com/enjoy-digital/litepcie\\_ptm\\_test](https://github.com/enjoy-digital/litepcie_ptm_test)

Thanks a lot to the great work of Florent from EnjoyDigital  


# How to get PCIe PTM on the Time Card?

AMD PHY workaround

- LitePCle wraps existing PHYs from FPGA vendors
- The Artix PHYs did not redirect the PTM TLP messages
- PCIePTMSniffer has been implemented:

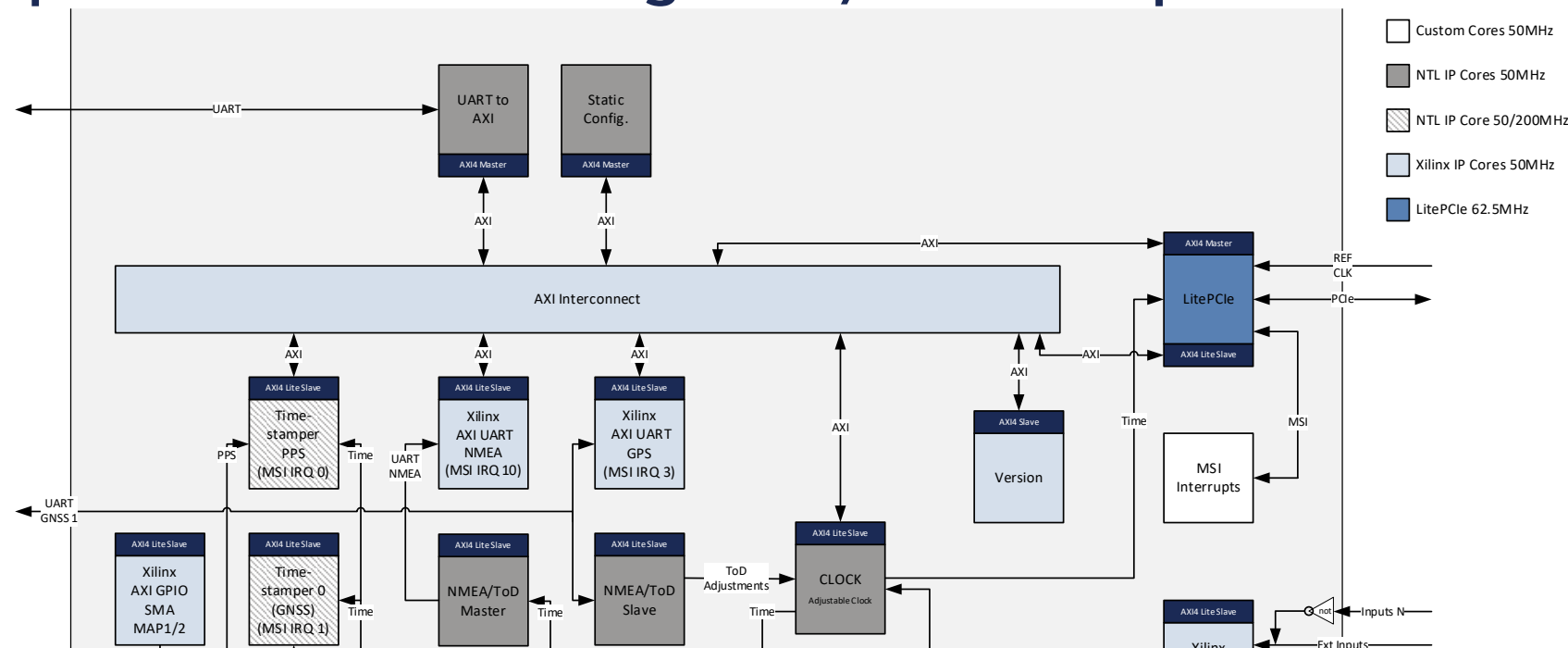


Picture Source: [https://github.com/enjoy-digital/litepcie\\_ptm\\_test](https://github.com/enjoy-digital/litepcie_ptm_test)

# How to get PCIe PTM on the Time Card?

Integration into the Time Card FPGA design

- LitePCle has a PTM Time Interface (Clk, Reset and Time in ns)
- LitePCle gets the time from the PHC of the Time Card
- LitePCle provides different registers/timestamps to handle PTM in the driver



# How to get PCIe PTM on the Time Card?

Integration into the Time Card Driver design

- **getcrosststamp calls syncdevicetime**
  - Trigger a PTM Request from the Time Card
  - Wait until the PTM State is not busy and the internal PTM Status becomes valid
  - Read  $t_1'$ , get  $t_2'$  and the propagation delay ( $t_3 - t_2$ ) from the PTM Response
  - Calculation of the PTM Master Time (@  $t_1'$ ):  $t_2' - \text{LinkDelay}$
  - Returned as Cross-Timestamp

- **PTM devices require hardware time stamping**
  - Time stamping of TLPs on transmission and reception
- **PTM-enabled Root Complex (PCIe host controller)**
- **Firmware and drivers that support PTM**
- **Application that uses it**

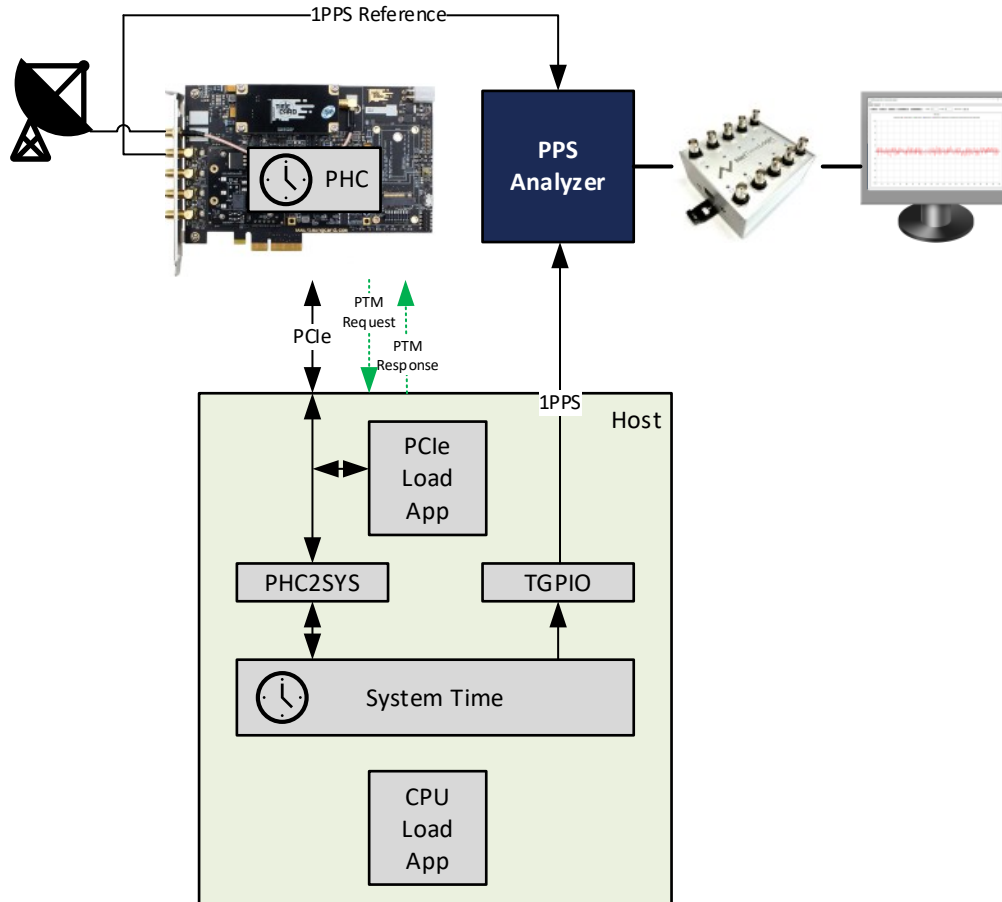
→ PCIe 3.0 or later is not really a requirement for the endpoint devices

- **Precise correlation of clocks within a platform**
  - Synchronize the host from a device
  - Synchronize a device from the host
- **Minimize the drift between devices**
- **Dynamic Time Adjustments**
  - e.g., with linuxptp phc2sys
- **Accurate latency measurement of the communication channel**

- **Reduced Timing Jitter in a system**
- **Improved Accuracy in a system**
- **Improved Determinism in a system**
- **Precise Cross-Device Synchronization**
  - PTM allows easy combination with PTP

# Measurements

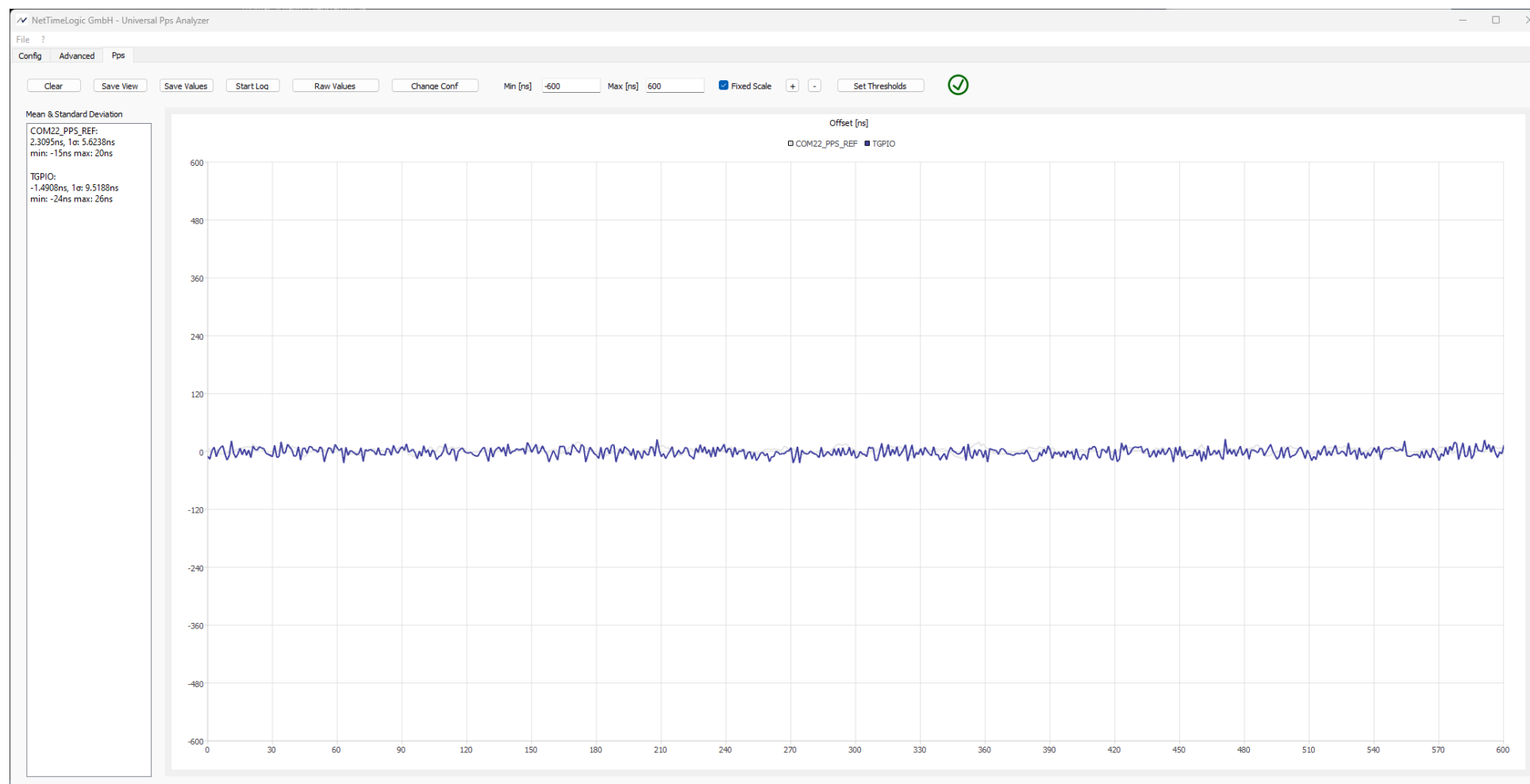
## Test Setup



- Measured 1PPS Ref Jitter: +/- 20ns
- Measurement Duration: 10 minutes
- PCIe Load App that reads a lot of registers on the Time Card
- CPU Load App that creates up to 100% CPU load
- linuxptp v4.3 was used
- App generates a 1PPS from the system time of the host and provides it to a TGPIO pin

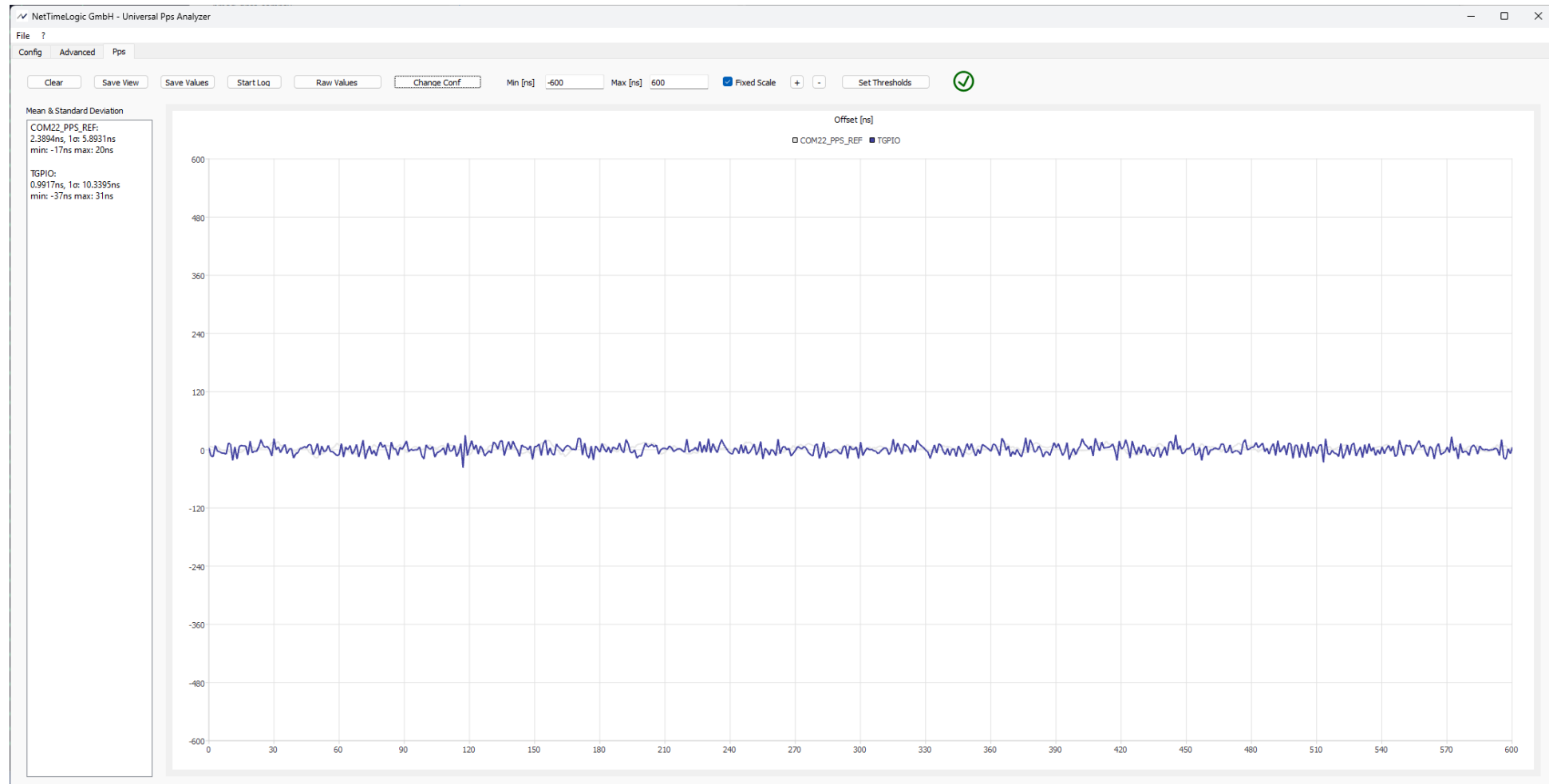
# Measurements

## Without PTM - No load on PCIe and CPU



# Measurements

With PTM - No load on PCIe and CPU



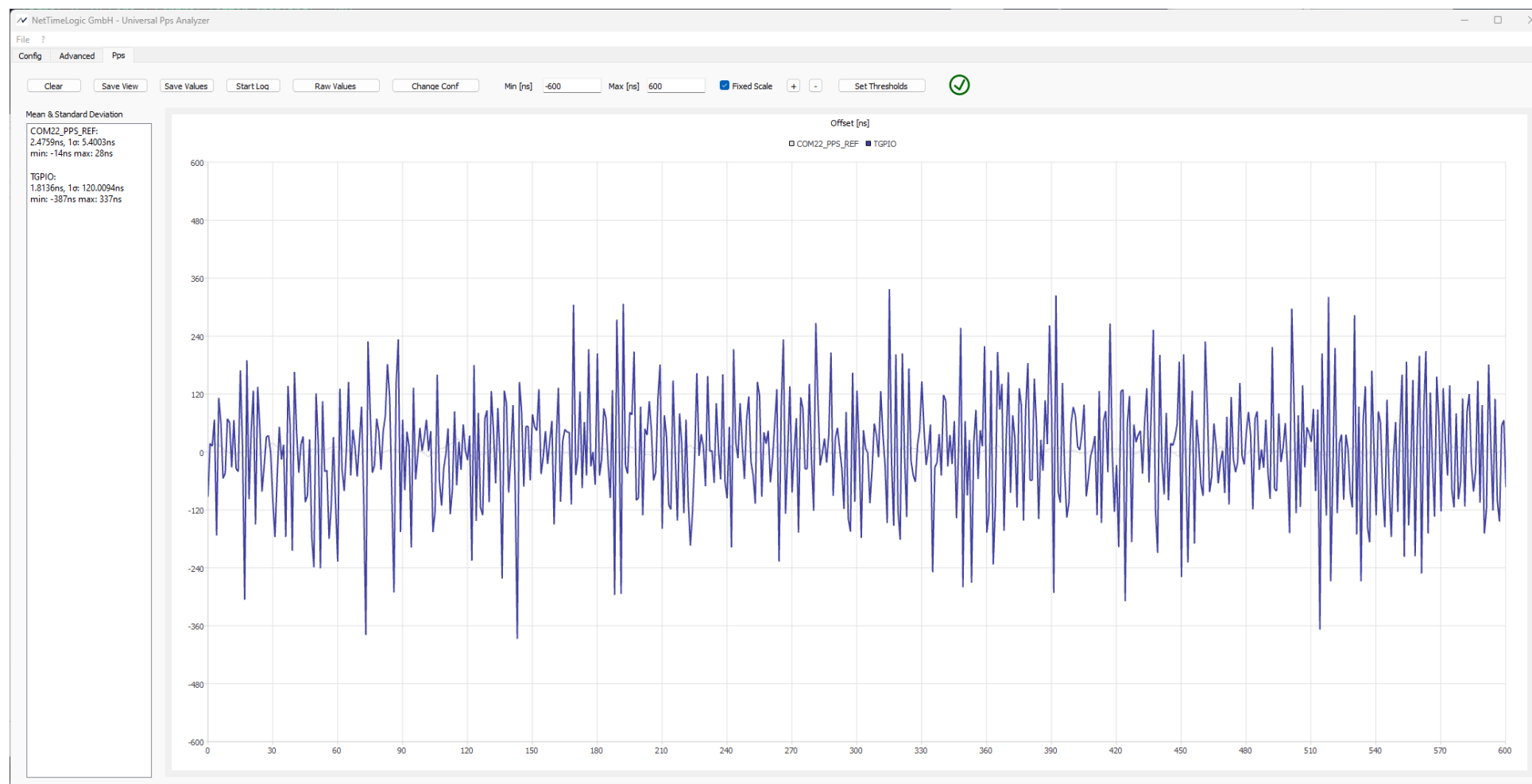
# Measurements

No load on PCIe and CPU

- No measurable difference between the version with PTM and without PTM support
- TGPIO Jitter:  $\sim \pm 30\text{ns}$
- PCIe without PTM support can achieve similar synchronization accuracy when almost no load is applied

# Measurements

## Without PTM - Load on PCIe and CPU



# Measurements

## With PTM - Load on PCIe and CPU



- **Without PTM support:**
  - TGPIO Jitter:  $> \pm 330\text{ns}$
- **With PTM support:**
  - TGPIO Jitter:  $\sim \pm 30\text{ns}$
  - Immunity against both kind of load
- **CPU load only does not really affect the synchronization accuracy with and without PTM**

- The measurement confirms the expectations
- The difference between PTM and no PTM support is not huge when there is no load
- With PTM we get immunity to load on the PCIe-Bus and on CPU load
- PTM support ensures that accuracy remains unaffected

- **Make Time Card FPGA Design available for all versions**
- **Deploy the Time Card with PTM**
  - Show the benefits of PTM
- **Mainline the PTM capable driver**
- **Promote the PCIe PTM capable LitePCIe solution for AMD FPGAs**
  - It is currently the only known solution for AMD FPGAs

## Thank you!

See Network Timing, Network Redundancy and our modular Hardware Platform AIONYX live at our booth!!!

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