TsnNetworkNode

A low-footprint, highly configurable, 100% hardware only IEEE 802.1 Time Sensitive Networking (TSN) solution, specifically designed for synchronous, deterministic, real-time and high-availability distributed systems. Allows running network redundancy, synchronization, scheduling, filtering, preemption, etc. completely independent and standalone from the user application.

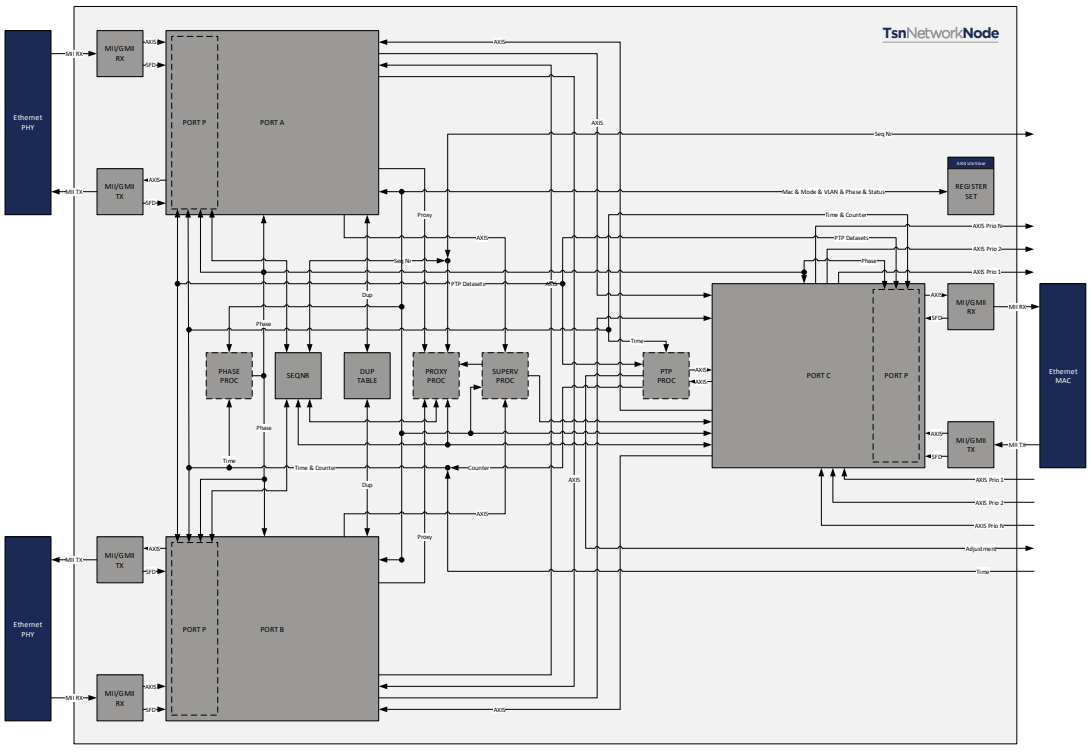
Key Features:

- 3 Port Switch
- Up to 8 AXI stream interfaces
- IEEE 802.1 AS, IEEE 1588
- IEEE 802.1 Qbu, IEEE 802.3 br
- IEEE 802.1 Qbv, IEEE 802.1 Qch
- IEEE 802.1 Qci
- IEEE 802.1 CB, IEC62439-3
- Full line speed frame handling
- 100% hardware only solution
- Supports up to 256 nodes on uplink
- Vendor independent

Typical Applications:

- Ethernet based automation networks
- High availability environments
- Substation automation
- Distributed data acquisition
- Robotic
- Automotive
- Test and measurement
- Etc.

IP Core Architecture:



Specification:

Switch Ports	Two forwarding ports, 1 internal/interlink port. Supports up to 256 MACs connected
Stream Inter-faces	Up to 8 AXI stream interfaces to send/receive real-time traffic to/from a specific priority/phase
IEEE 802.1 AS, IEEE 1588	Synchronization with sub-microsecond accuracy which allows time driven scheduling and cycles
IEEE 802.1 Qbu, IEEE 802.3 br	Frame preemption can be enabled for the lowest priority class to allow for minimum sized save guards, which allows maximum bandwidth usage
IEEE 802.1 Qbv, IEEE 802.1 Qch	Frame scheduling, up to 8 different phases within each cycle, cycle time as well as assigned VLAN priorities can be freely chosen. Cyclic forwarding can be enabled to have a complete deterministic forwarding behavior.
IEEE 802.1 CB, IEC62439-3	Parallel Redundancy Protocol (PRP) and High Availability Seamless Redundancy (HSR) with ModeH and optional ModeX IEEE 802.1 Frame Replication & Elimination for Reliability.
Performance	Full line speed frame handling,
Portability	100% hardware only solution, no dependency on external CPU Vendor independent, written in plain VHDL Low footprint and low frequency requirements
Modularity	Slim and standardized interfaces are used
Configuration	No CPU required, standalone configuration with signals Axi4 lite slave support, for status and configuration

Deliverables:

- Ip core in plain VHDL
- Testbench in plain VHDL
- Reference Design
  - Top level VHDL file
  - Timing Constraint SDC files
  - Vivado/Quartus Project file

Related Products:

- PTP Transparent Clock
- PTP Ordinary Clock
- PTP Hybrid Clock
- RED HSR & PRP

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