TsnEndNode

A low-footprint, highly configurable, 100% hardware only IEEE 802.1 Time Sensitive Networking (TSN) End Node solution, specifically designed for synchronous, deterministic, real-time and high-availability distributed systems. Allows running nsynchronization, scheduling, filtering, preemption, etc. completely independent and standalone from the user application and can be connected to any MAC.

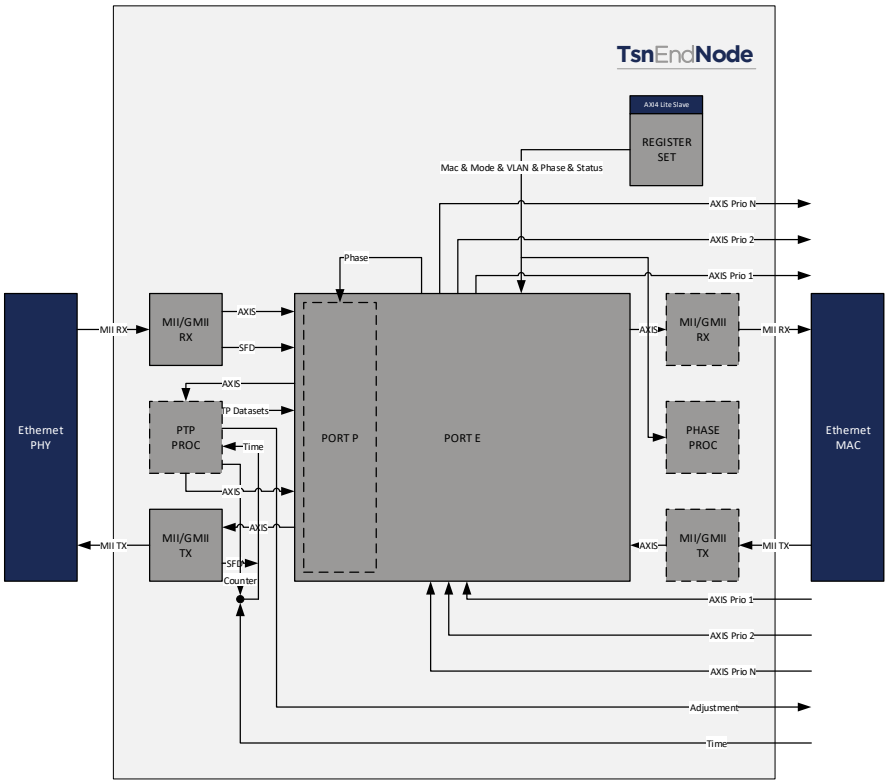
Key Features:

- 1 Port, between MAC and PHY
- Up to 8 AXI stream interfaces
- IEEE 802.1 AS, IEEE 1588
- IEEE 802.1 Qbu, IEEE 802.3 br
- IEEE 802.1 Qbv, IEEE 802.1 Qch
- IEEE 802.1 Qav
- Full line speed frame handling
- 100% hardware only solution
- Vendor independent

Typical Applications:

- Ethernet based automation networks
- Substation automation
- Distributed data acquisition
- Robotic
- Automotive
- Test and measurement
- Etc.

IP Core Architecture:



Specification:

Forwarding-Port	Forwarding port between MAC and PHY, can be connected to any MAC, also retrofits existing CPU/MAC design
Stream Inter-faces	Up to 8 AXI stream interfaces to send/receive real-time traffic to/from a specific priority/phase
IEEE 802.1 AS, IEEE 1588	Synchronization with sub-microsecond accuracy which allows time driven scheduling and cycles
IEEE 802.1 Qbu, IEEE 802.3 br	Frame preemption can be enabled for the lowest priority class to allow for minimum sized save guards, which allows maximum bandwidth usage
IEEE 802.1 Qbv, IEEE 802.1 Qch	Frame scheduling, up to 8 different phases within each cycle, cycle time as well as assigned VLAN priorities can be freely chosen. Cyclic forwarding can be enabled to have a complete deterministic forwarding behavior.
IEEE 802.1 Qav	Credit based traffic shaping for each priority.
Performance	Full line speed frame handling,
Portability	100% hardware only solution, no dependency on external CPU Vendor independent, written in plain VHDL Low footprint and low frequency requirements
Modularity	Slim and standardized interfaces are used
Configuration	No CPU required, standalone configuration with signals Axi4 lite slave support, for status and configuration

Deliverables:

- Ip core in plain VHDL
- Testbench in plain VHDL
- Reference Design
  - Top level VHDL file
  - Timing Constraint SDC files
  - Vivado/Quartus Project file

Related Products:

- PTP Transparent Clock
- PTP Ordinary Clock
- PTP Hybrid Clock
- RED TSN Network Node

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