PtpServer

A low-footprint, configurable, 100% hardware only CSPTP Server solution based on the first draft of the upcoming CSPTP standard (Client-Server-PTP, IEEE 1588.1), specifically designed for high-performance distributed systems, datacenters and time servers. Allows running PTP synchronization completely independent and standalone from the user application with the highest performance on the market

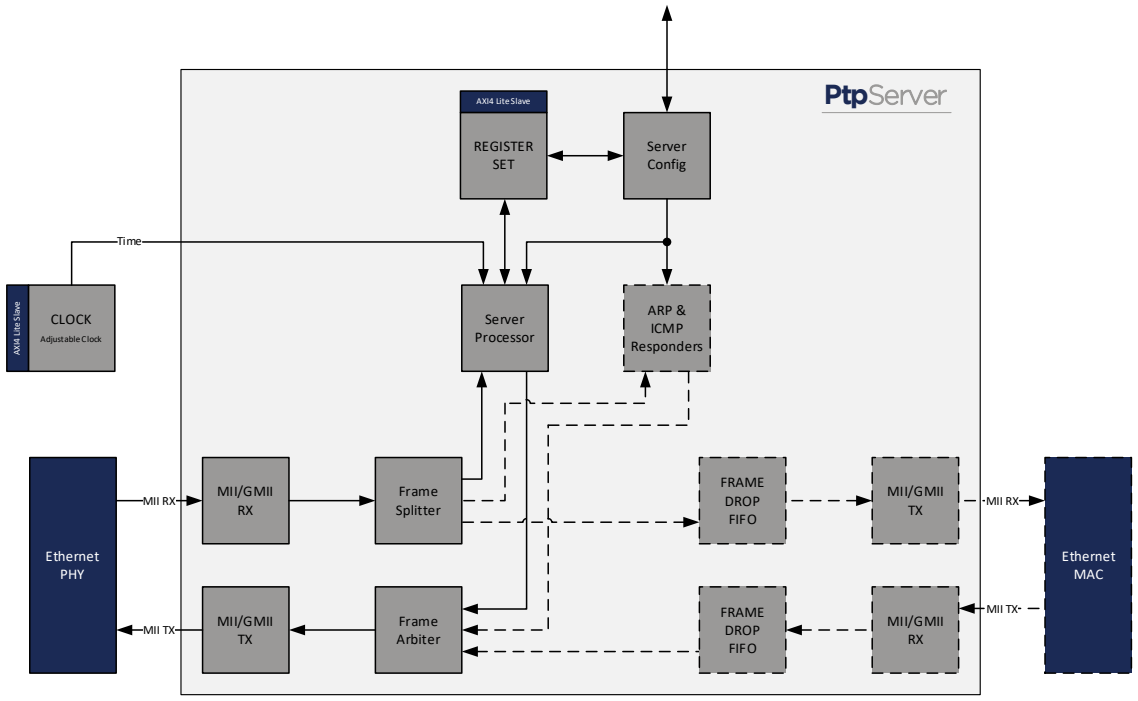
Key Features:

- PTP Server according to PTPv2.1 (IEEE1588) and the first Draft of CSPTP (IEEE1588.1)
- One-Step operation (can handle Two-Step requests)
- P2P Support
- 100% hardware only solution
- Vendor independent
- Full line speed, handling ~1mio requests/s @ 1000Mbit/s

Typical Applications:

- High Performance PTP Server
- Ethernet based automation net-works
- Power and Utilities
- Distributed data acquisition
- Datacenters
- Test and measurement
- Etc.

IP Core Architecture:



Specification:

CSPTP IEEE1588 IEEE1588.1	According to the first draft of CSPTP (IEEE1588.1) specification Support for One-Step operation as Client and supports One- and Two-Step operating Servers, support for Layer2, Ipv4, IPv6 Support for P2P. Flexible configuration
Performance	Full line speed, handling ~1mio requests/s @ 1000Mbit/s, offloading synchronization, delivers the highest performance with minimal resources Hardware timestamping with 4ns resolution
Portability	10/100/1000 Mbit/s support, intercepts (R)(G)MII interfaces between MAC and PHY (no MAC required) 100% hardware only solution, no dependency on external CPU or PHY features Vendor independent, written in plain VHDL Low footprint and low frequency requirements
Accuracy	Sub-microsecond accuracy on a PTP aware network 4ns Timestamps accuracy
Modularity	Modular system; adjustable clock is a separate core which can be also synchronized to another source (GPS, DCF, etc.) Slim and standardized interfaces are used
Configuration	No CPU required, standalone configuration with signals Axi4 lite slave support, for status and configuration

Deliverables:

- Ip core in plain VHDL
- Testbench in plain VHDL
- Reference Design
  - Top level VHDL file
  - Timing Constraint SDC files
  - Vivado/Quartus Project file

Related Products:

- TOD Slave
- DCF Slave
- Adjustable Clock
- PPS Master/Slave
- IRIG Master/Slave
- Signal Timestamper
- Signal Generator

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