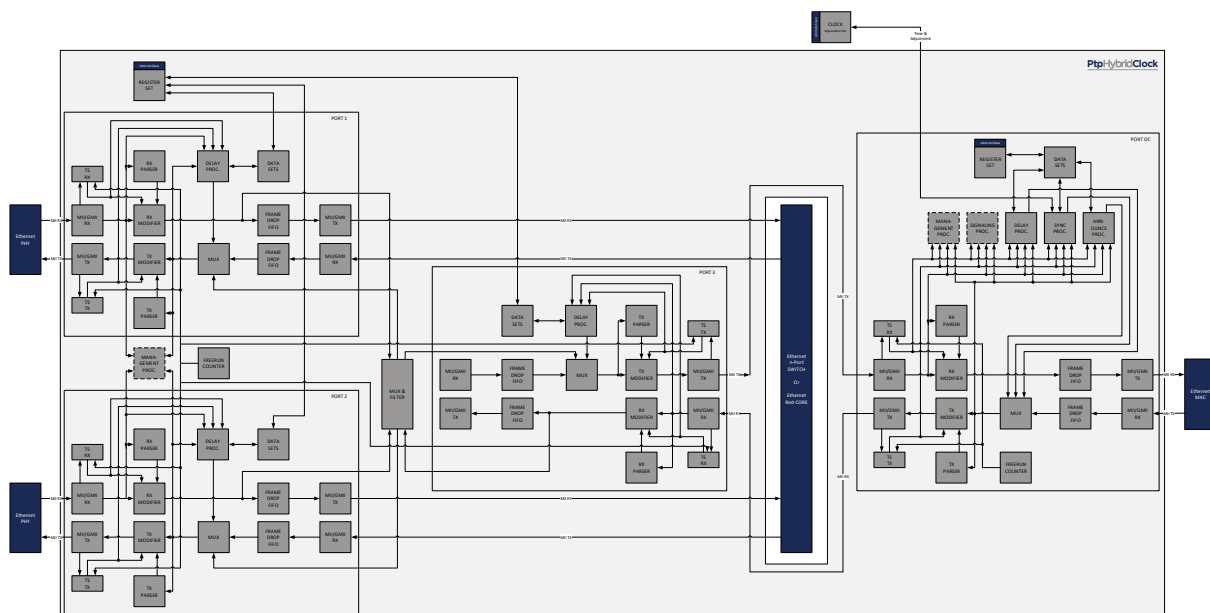


Key Features:

- ## Typical Applications:

- ## IP Core Architecture:



Specification:

IEEE1588	Layer 2 and Ipv4, P2P/E2E delay mechanism, 1 step hybrid clock, Master and Slave capability, multicast and unicast 2 port daisy chain, OC is able to send and receive from both ports, built out of a combination of NetTimeLogic's OC and TC Default-, Power-, Utility-, TSN- and ITU-profile support Complete Dataset support PTP Management message support Offset and drift calculation for adjusting the clock
Performance	Full line speed frame handling, offloading synchronization 10/100/1000 Mbit/s support, intercepts (R)(G)MII interfaces between MAC and PHY or an Ethernet Switch (no MAC required)
Portability	100% hardware only solution, no dependency on external CPU or PHY features Vendor independent, written in plain VHDL Low footprint and low frequency requirements
Accuracy	Sub microsecond synchronization With 50ppm Oscillator: +/- 100ns
Modularity	Modular system; adjustable clock is a separate core Slim and standardized interfaces are used, scalable to more ports
Configuration	No CPU required, standalone configuration with signals Axi4 lite slave support, for status and configuration

Deliverables:

- Ip core in plain VHDL
- Testbench in plain VHDL
- Reference Design with 2 ports for daisy chaining
 - Top level VHDL file
 - Timing Constraint SDC files
 - Vivado/Quartus Project file

Related Products:

- | | |
|-------------------------|----------------------|
| • PTP Ordinary Clock | • IRIG Master/Slave |
| • PTP Transparent Clock | • Adjustable Clock |
| • PTP Grandmaster Clock | • Signal Timestamper |
| • PPS Master/Slave | • Signal Generator |



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