

PmEth

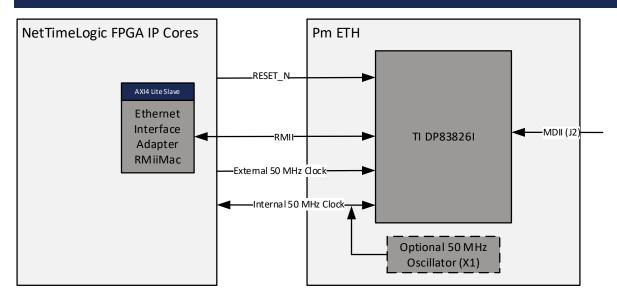
This Pmod[™] compatible module features an integrated PHY and RJ45 connector, providing up to 100Mbit/s Ethernet connectivity. Designed for easy integration, it connects directly to systems with a Pmod[™] connectors, enabling rapid networking capabilities.

Key Features:

- Up to 100Mbit/s Ethernet Connectivity via RMII interface
- RJ45 Connector
- Plug-and-Play: PHY is preconfigured via strapping pins
- Compact Design
- Versatile Applications
- Optionally configurable via strapping pins (solder option)



Block Diagram:



Specification:				
PHY		Texas Instruments DP83826I		
ETH	Connector	RJ45 (8P8C)		
		Green LED: Link status and activity		
		Orange LED: Link speed		
		o On: Link is 100 M		
<u> </u>	c:			
Cont	пg	Soldered strapping configuration (default):		
		R5 (1.5 kOhm) assembled: Full-Duplex		
		R9 (1.5 kOhm) not assembled: 100 M		
		R10 (1.5 kOhm) not assembled: AN ON		
		R4 (0 Ohm) not assembled: 50MHz PHY from external		
Pow	er	~45mA @ 3.3V		
Dm	od TM Dinc on	d Module Overview:		
	F, P	M ETH J2 1 − 7 2 − 8 IC1 IC1		
		M ETH . J2		
Pin	Signal	M ETH 1 7 2 8 4 10 5 11 R10 6 12		
Pin		tertimeLogic birection Description Header J1 (Pmod [™])		
		I J2 1 7 2 8 3 9 4 10 5 11 8 89 6 12 NetTimeLogic Direction Description Header J1 (Pmod™) EXT: In Clock for the PHY (Pin 9)		
	Signal	I I J 1 I I 2 8 I 3 9 I 4 10 I 5 11 R10 6 12 R9 6 10 R9 Header J1 (Pmod [™]) R0 EXT: In INT: Out Clock for the PHY (Pin 9) . External: If PmEth does not use the oscillator (X1) (default)		
1	Signal EXT/INT CLK	I 7 J2 8 IC1 3 9 IC1 IC1 4 10 IC1 IC1 5 11 R10 IC1 6 12 IC1 IC1 NetTimeLogic IC1 IC1 IC1 Direction Description Header J1 (Pmod™) EXT: In Clock for the PHY (Pin 9) IC1 INT: Out Clock for the PHY (Pin 9) IC1 INT: Out Internal: If PmEth does not use the oscillator (X1) (default) Internal: If PmEth use the oscillator (X1) Internal: If PmEth use the oscillator (X1)		
1 2	Signal EXT/INT CLK RX D1	I 7 10		
1 2 3	Signal EXT/INT CLK RX D1 CRS DV	I J2 I Header J1 (Pmod TM) I External: If PmEth does not use the oscillator (X1) (default) I Internal: If PmEth use the osc		
1 2 3 4	Signal EXT/INT CLK RX D1 CRS DV TX D1	I 7 10		
1 2 3	Signal EXT/INT CLK RX D1 CRS DV	ETH J2 2 8 3 9 4 10 5 11 8 R10 6 12 NetTimeLogic Direction Description Header J1 (Pmod TM) EXT: In Clock for the PHY (Pin 9) INT: Out External: If PmEth does not use the oscillator (X1) (default) 0ut RMII Reception Data 1 Pin of the PHY (Pin 15) Out RMII Carrier and Receive Data Valid indicator of the PHY (Pin 18) In RMII Transmission Data 1 Pin of the PHY (Pin 25) In RMII Transmission Data 1 Pin of the PHY (Pin 25) GND connection to the carrier board		
1 2 3 4 5	Signal EXT/INT CLK RX D1 CRS DV TX D1 GND	I J2 I IC1 I IC1 <		

		3.3V supply from the carrier board		
RJ45				
	In/Out	RJ45 (8P8C) connector for Ethernet connectivity up to 100 Mbit/s		



TX EN

TX D0

GND

VCC

RJ45

In

In

9

10

11

12

J2

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RMII Transmission Enable of the PHY (Pin 23)

GND connection to the carrier board

RMII Transmission Data O Pin of the PHY (Pin 24)