NtpServerClock

Reference Manual

Product Info	
Product Manager	Sven Meier
Author(s)	Thomas Schaub, Sven Meier
Reviewer(s)	Sven Meier
Version	1.2
Date	16.02.2024

Copyright Notice

Disclaimer

The information available to you in this document/code may contain errors and is subject to periods of interruption. While NetTimeLogic GmbH does its best to maintain the information it offers in the document/code, it cannot be held responsible for any errors, defects, lost profits, or other consequential damages arising from the use of this document/code.

NETTIMELOGIC GMBH PROVIDES THE INFORMATION, SERVICES AND PRODUCTS AVAILABLE IN THIS DOCUMENT/CODE "AS IS," WITH NO WARRANTIES WHATSOEVER. ALL EXPRESS WARRANTIES AND ALL IMPLIED WARRANTIES, INCLUDING WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF PROPRIETARY RIGHTS ARE HEREBY DISCLAIMED TO THE FULLEST EXTENT PERMITTED BY LAW. IN NO EVENT SHALL NETTIMELOGIC GMBH BE LIABLE FOR ANY DIRECT, INDIRECT, INCIDENTAL, CONSEQUENTIAL, SPECIAL AND EXEMPLARY DAMAGES, OR ANY DAMAGES WHATSOEVER, ARISING FROM THE USE OR PERFORMANCE OF THIS DOCUMENT/CODE OR FROM ANY INFORMATION, SERVICES OR PRODUCTS PROVIDED THROUGH THIS DOCUMENT/CODE, EVEN IF NETTIMELOGIC GMBH HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

IF YOU ARE DISSATISFIED WITH THIS DOCUMENT/CODE, OR ANY PORTION THEREOF, YOUR EXCLUSIVE REMEDY SHALL BE TO CEASE USING THE DOCUMENT/CODE.

Overview

NetTimeLogic's NTP Server is a full hardware (FPGA) only implementation of a Simple Network Time Protocol v4 (SNTP) Server according to RFC 4330/5905. The whole protocol handling, algorithms and calculations are implemented in the core, no CPU is required. This allows running a NTP Server completely independent and standalone from the user application. The NTP Server can act as a Unicast or Broadcast Server and is able to handle line speed requests (100k+, ~500k). The server can be configured either by signals or by an AXI4Lite-Slave Register interface.

Key Features:

- SNTP Server according to RFC 4330/5905
- Intercepts path between MAC and PHY
- Single Port
- Support for Unicast, Multicast or Broadcast
- Full line speed, handling 100k+ (~500k) requests
- Hardware timestamping on ®(G)MII level
- Support for UTC leap second handling (jump or smearing),
- Optional leap second smearing (configurable rate)
- AXI4Lite register set or static configuration
- MII/GMII/RGMII Interface support (optional AXI4 stream for interconnection to 3rd party cores)
- Timestamp resolution with 50 MHz system clock: 10ns or with a 250MHz aligned clock 4ns
- Hardware PI Servo

Revision History

This table shows the revision history of this document.

Version	Date	Revision
0.1	17.09.2021	First draft
1.0	27.09.2021	First release after review
1.1	03.01.2023	Added Vivado upgrade version description
1.2	16.02.2024	IPv6 added

Table 1: Revision History

Content

Definitions

Definitions	
Client	The NTP Device which requests the time from the Server
Server	The NTP Device answering requests

Table 2: Definitions

Abbreviations

Abbreviations	
AXI	AMBA4 Specification (Stream and Memory Mapped)
CRC	Cyclic Redundancy Check
ETH	Ethernet
FF	Flip Flop
FPGA	Field Programmable Gate Array
IP	Internet Protocol
IRQ	Interrupt, Signaling to e.g. a CPU
LUT	Look Up Table
MAC	Media Access Controller
NTP	Network Time Protocol
PHY	Physical Media Access Controller
RAM	Random Access Memory
ROM	Read Only Memory
SNTP	Simple Network Time Protocol
TB	Testbench
TS	Timestamp
UDP	User Datagram Protocol
VHDL	Hardware description Language for FPGA's

Table 3: Abbreviations

1 Introduction

1.1 Context Overview

The NTP Server (SNTP Server) is meant as a co-processor handling NTP requests. It intercepts the Media Independent Interface (MII) on the Ethernet path between the MAC and PHY where it handles all NTP traffic. This means it generates and processes NTP frames directly in hardware, using the same data path as the normal traffic coming from or going to the Ethernet MAC. The NTP Server is designed to work in cooperation with the Counter Clock core from NetTimeLogic (not a requirement). It contains an AXI4Lite slave for configuration from a CPU, this is however not required since the NTP Server can also be configured statically via signals/constants directly from within the FPGA.

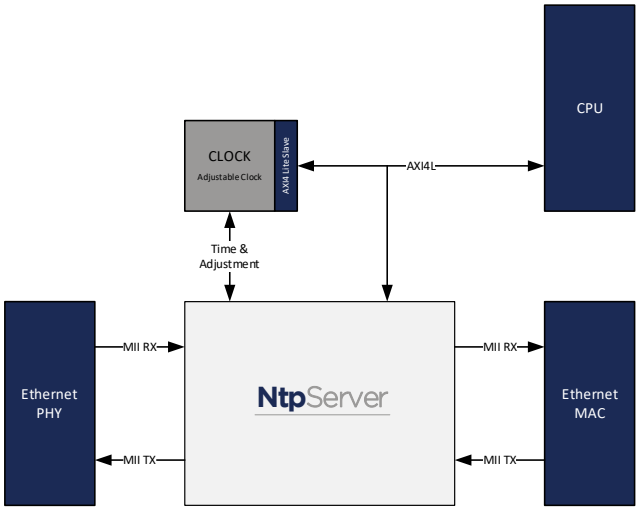

Figure 1: Context Block Diagram

1.2 Function

The NTP Server is a SNTP v4 Server according to RFC 4330/5905. As a server it provides an accurate time to NTP clients. The accurate time is given from the Counter Clock which can be also the sink of an external reference time source like GNSS, DCF77 or something similar.
The server supports different modes, either with responses to requests of a client or sending directly the time using broadcast. The IP Core can act as an endpoint which fully handles NTP or it can also work in a throughput mode where it does handle NTP frames but all other traffic goes through the Core.

1.3 Architecture

The core is split up into different functional blocks for reduction of the complexity, modularity and maximum reuse of blocks. The interfaces between the functional blocks are kept as small as possible for easier understanding of the core.

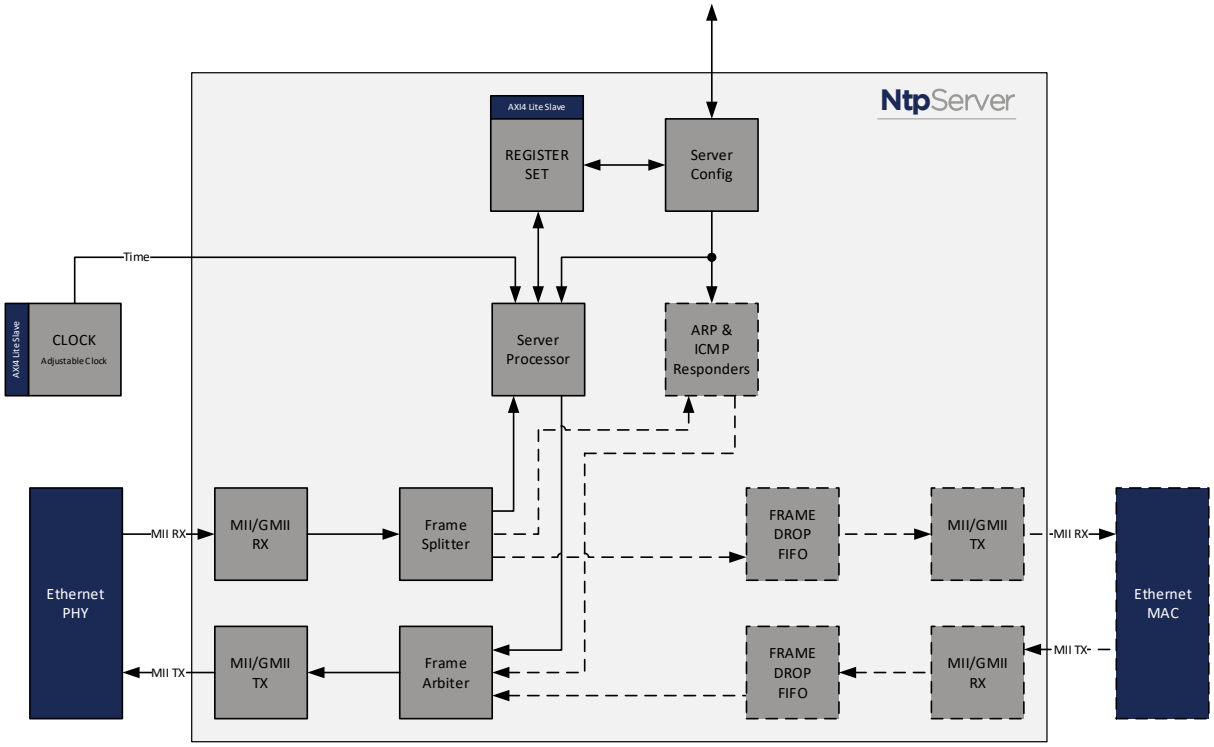

Figure 2: Architecture Block Diagram

Register Set

This block allows reading status values and writing configuration.

Server Config

This block stores the configuration of the server. There are multiple sources possible, like the configuration via the register set, static configuration from externally or also UTC information from externally.

Server Processor

This block is the heart the NTP Server. The Server Processor timestamps the incoming frames, extracts the information of the NTP request and stores this information in a frame information FIFO. With the data from this FIFO the frame creator generates the response which includes the transmit timestamp. Depending on the selected mode also the NTP broadcast frames are generated by the Server Processor. Additionally, UTC handling is done by the Server Processor block.

ARP & ICMP Responder

These modules answers ARP or ICMP requests with ARP or ICMP responses.

Frame Splitter

This module splits one AXIS interface to multiple, allowing the ARP Responder to receive ARP requests, forwarding frames through the core and forward frames to the server processor

Frame Arbiter

This module arbitrates multiple AXIS interfaces to one, allowing the ARP Responder to answer ARP requests, forwarding frames through the core and sending NTP messages from the server processor.

Frame Drop Fifo

This FIFO is a store and forward FIFO with drop functionality. During frame reception a drop signal can be asserted which will cause that the frame is dropped. If it will run into an overflow condition it drops the incoming frame.

(R)(G)MII Receive/Transmit Interface Adapter

These blocks convert the data stream from the (R)(G)MII to a 32bit AXI stream and back from 32bit AXI stream to (R)(G)MII.

2 NTP Basics

2.1 Protocol

NTP means Network Time Protocol and it is a protocol to synchronize device clocks over a network to a reference time base. The protocol exists since 1985 and it is specified in several Request for Comments (RFC). The most recent and relevant ones are RFC 5905 (NTPv4) and RFC 4430 (SNTPv4). NTP is built on the Internet Protocol (IP)and the User Datagram Protocol (UDP).
The principal of the protocol is based on periodically request from a client to the server for the precise UTC time reference. In the client-server mode the NTP server is listening for NTP packets on UDP port 123 and replies to these packets. NTP does also have a broadcast variant where the server sends periodically packets that can be received by multiple clients (but without the possibility to compensate for path delays).

2.2 Principles

The basic operation of NTP is timestamping of data packets transferred between the server and the client. The NTP packets sent from a client to the server and the responses from the server to the client have the same format. The server fills fields such as timestamps to the received packet and sends it back to the clients.

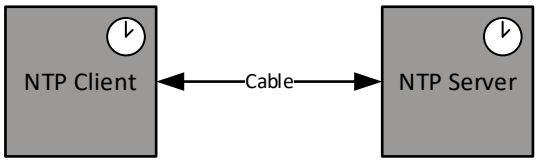

Figure 3: Simple setup

The NTP packet consists of four timestamps. The timestamps are 64 bits with 32 bits as second and 32 bits as fraction:

- Reference timestamp: Time when the system clock was last set
- Origin timestamp: Time at the client when the request departed
- Receive timestamp: Time at the server when the request arrived
- Transmit timestamp: Time at the server when the response left

The client sends the request to the server with the origin timestamp (T1). The server takes a timestamp of the time when the request packet is received (receive timestamp T2). The server sends the response packet back to the client with the

transmit timestamp (T3). The client stamps the time when the response packet is received (destination timestamp T4).

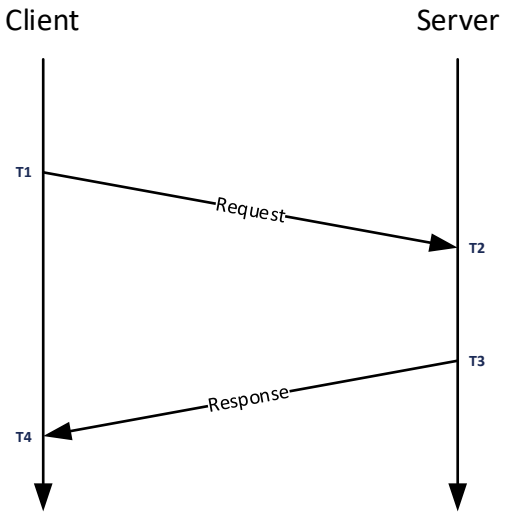

Figure 4: Message exchange simple setup

With these timestamps the offset and the roundtrip delay can be calculated:

$$Offset = \frac{(T2 - T1) + (T3 - T4)}{2}$$

$$Delay = (T4 - T1) - (T3 - T2)$$

In Broadcast mode, the fields origin timestamp and receive timestamp are by convention set to zero.

2.3 Accuracy

The accuracy of the synchronization depends mostly on the jitter of the network between the Client and Server but also highly on the precision of the timestamps. They should reflect the send and receive time as precise as possible. The client's Offset and Delay calculations are based on the difference of timestamps taken at two different places.

The achievable accuracy depends on:

- Network Jitter
- Network Symmetry
- Timestamp accuracy
- Clock stability

- Clock control loop characteristics
- Drift compensated clocks (i.e. adjusted time base of the Server)

2.3.1 Network jitter and symmetry

The accuracy of an NTP system is heavily dependent on a symmetrical jitter free network path between the client and the master. However, since this is never the case advanced filtering is required to get a good mean value and filter out outliners. It is aways important to know that it is always a tradeoff between fast synchronization and accuracy/stability. Also, a quite jittery network will lead to a long-term stable system but short-term fluctuations.
Since for the offset calculation a symmetrical link is required (division by 2) any asymmetry will directly result in an offset which is hard to mitigate since paths can change at every moment.

2.3.2 Timestamp accuracy

As just stated, timestamp accuracy is the key to high accuracy. Timestamp support can be implemented at different layers with a decrease in accuracy in the higher layers. For this solution a timestamp point between MAC and PHY (on MII) was chosen to get the best possible accuracy without implementing PHY functionality This interface is perfect for the use of FPGAs since it is a strictly digital interface, standardized and has only a low frequency requirement. For this implementation the FPGA is intercepting the Path between MAC and PHY.

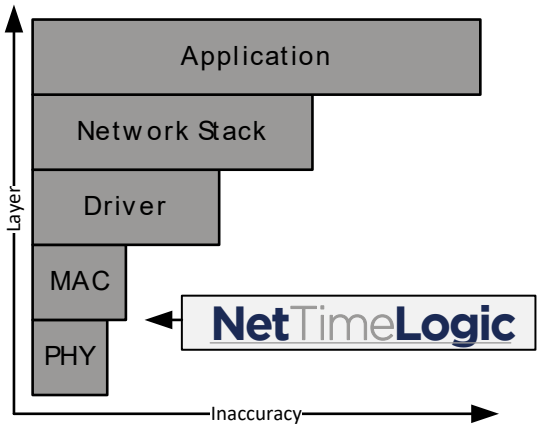

Figure 5: Timestamp Inaccuracy in the different Layers

Not only timestamping but also frame generation, handling and servo loops can be done in different stages. A wide spread approach is to have the timestamping at a very low layer and all other things in the application layer which implies that a MAC,

CPU and Operating System with Drivers a Network Stack and a NTP application is in place. NetTimeLogic's approach is different: NetTimeLogic's NTP Server is completely implemented in an FPGA meaning that all the upper layers after the PHY are not required. This decreases the complexity and dependencies between the different layers and allows running the system without CPU. It also allows to answer request at line speed

2.4 Difference between SNTP and NTP

Simple Network Time Protocol (SNTP) is a stripped-down version of NTP. SNTP and NTP share several similarities. The packets of data exchanged between the clients and the server are identical, which makes any time server compatible with both. The differences between NTP and SNTP is only affecting the synchronization on the client side.
The main difference is that no mitigation algorithms are implemented. In addition, SNTP is intended for primary server equipped with a single reference clock, so it is based on a single server-client relationship.

3 Register Set

This is the register set of the NTP Server. It is accessible via AXI4Lite Memory Mapped. All registers are 32bit wide, no burst access, no unaligned access, no byte enables, no timeouts are supported. Register address space is not contiguous. Register addresses are only offsets in the memory area where the core is mapped in the AXI inter connects. Non existing register access in the mapped memory area is answered with a slave decoding error.

3.1 Register Overview

Registerset Overview			
Name	Description	Offset	Access
Ntp ServerControl Reg	NTP Server Enable Control Register	0x00000000	RW
Ntp ServerStatus Reg	NTP Server Error Status Register	0x00000004	WC
Ntp ServerVersion Reg	NTP Server Version Register	0x0000000C	RO
Ntp ServerCountControl Reg	NTP Server Count Control Register	0x00000010	RW
Ntp ServerCountReq Reg	NTP Server Request Count Register	0x00000014	RO
Ntp ServerCountResp Reg	NTP Server Response Count Register	0x00000018	RO
Ntp ServerCountReqDropped Reg	NTP Server Request Dropped Count Register	0x0000001C	RO
Ntp_ServerCountBroadcast_Reg	NTP Server Broadcast Count Register	0x00000020	RO
Ntp ServerConfigControl Reg	NTP Server Configuration Control Register	0x00000080	RW
Ntp ServerConfigMode Reg	NTP Server Configuration Mode Register	0x00000084	RW
Ntp ServerConfigVlan Reg	NTP Server Configuration VLAN Register	0x00000088	RW
Ntp ServerConfigMac1 Reg	NTP Server Configuration MAC 1 Register	0x0000008C	RW
Ntp ServerConfigMac2 Reg	NTP Server Configuration MAC 2 Register	0x00000090	RW
Ntp ServerConfigIp Reg	NTP Server Configuration IPv6 0 and Ipv4 Register	0x00000094	RW
Ntp ServerConfigIpv61 Reg	NTP Server Configuration IPv6 1 Register	0x00000098	RW
Ntp ServerConfigIpv62 Reg	NTP Server Configuration IPv6 2 Register	0x0000009C	RW

Ntp ServerConfigIpv63 Reg	NTP Server Configuration IPv6 3 Register	0x000000A0	RW
Ntp ServerReferenceId Reg	NTP Server Configuration IPv6 3 Register	0x000000A4	RW
Ntp ServerUtcInfoControl Reg	NTP Server UTC Info Control Register	0x00000100	RW
Ntp ServerUtcInfo Reg	NTP Server UTC Info Register	0x00000104	RW

Table 4: Register Set Overview

3.2 Register Descriptions

3.2.1 General

3.2.1.1 NTP Server Control Register

Used for general control over the NTP Server.

Ntp ServerControl Reg																													
Reg Description																													
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RO																															RW
ENABLE																															
Reset: 0x00000000																															
Offset: 0x0000																															

Name	Description	Bits	Access
-	Reserved, read 0	Bit:31:1	RO
ENABLE	Enable	Bit: 0	RW

3.2.1.2 NTP Sever Status Register

Shows the current status of the NTP Server.

Ntp ServerStatus Reg																													
Reg Description																													
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
																															ERROR
RO																															WC
Reset: 0x00000000																															
Offset: 0x0004																															

Name	Description	Bits	Access
-	Reserved, read 0	Bit:31:1	RO
ENABLE	Error (sticky)	Bit: 0	WC

3.2.1.1 NTP Version Register

Version of the IP core, even though is seen as a 32bit value, bits 31 down to 24 represent the major, bits 23 down to 16 the minor and bits 15 down to 0 the build numbers.

Ntp ServerVersion Reg																													
Reg Description																													
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VERSION																													
RO																													
Reset: 0xXXXXXXXX																													
Offset: 0x000C																													

Name	Description	Bits	Access
VERSION	Version of the IP core	Bit: 31:0	RO

3.2.1.2 NTP Server Count Control Register

Used for clearing all statistic counters

Ntp ServerCountControl Reg																													
Reg Description																													
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
																															CLEAR
RO																															RW
Reset: 0x00000000																															
Offset: 0x0010																															

Name	Description	Bits	Access
-	Reserved, read 0	Bit:31:1	RO
CLEAR	Clear all counters (self cleared)	Bit: 0	RW

3.2.1.3 NTP Server Count Request Registers

Received number of NTP Requests.

Ntp ServerCountReq Reg																													
Reg Description																													
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RX_REQ																													
RO																													
Reset: 0x00000000																													
Offset: 0x0014																													

Name	Description	Bits	Access
RX_REQ	Received number of NTP requests	Bit: 31:0	RO

3.2.1.4 NTP Server Count Response Registers

Sent number of NTP Responses.

Ntp ServerCountResp Reg																													
Reg Description																													
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TX_RESP																													
RO																													
Reset: 0x00000000																													
Offset: 0x0018																													

Name	Description	Bits	Access
TX_RESP	Sent number of NTP responses	Bit: 31:0	RO

3.2.1.5 NTP Server Count Request Dropped Registers

Number of dropped NTP Requests.

Ntp ServerCountReqDropped Reg																													
Reg Description																													
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REQ_DROPPED																													
RO																													
Reset: 0x00000000																													
Offset: 0x001C																													

Name	Description	Bits	Access
REQ_DROPPED	Number of dropped requests	Bit: 31:0	RO

3.2.1.6 NTP Server Count Broadcast Registers

Number of sent broadcast NTP Packets.

Ntp ServerCountBroadcast Reg																													
Reg Description																													
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BROADCAST																													
RO																													
Reset: 0x00000000																													
Offset: 0x0020																													

Name	Description	Bits	Access
BROADCAST	Number of NTP broadcasts	Bit: 31:0	RO

3.2.1.7 NTP Server Configuration Control Register

Valid flags of the configuration of the NTP server.

Ntp ServerConfigControl Reg																														
Reg Description																														
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
																											REF_ID_VAL	IP_VAL	MAC_VAL	VLAN_VAL	MODE_VAL
RO																											RW	RW	RW	RW	RW
Reset: 0x00000000																														
Offset: 0x0080																														

Name	Description	Bits	Access
-	Reserved, read 0	Bit:31:5	RO
REF_ID_VAL	Reference ID valid (autocleared)	Bit: 4	RW
IP_VAL	IP valid (autocleared)	Bit: 3	RW
MAC_VAL	MAC valid (autocleared)	Bit: 2	RW
VLAN_VAL	VLAN valid (autocleared)	Bit: 1	RW
MODE_VAL	Mode valid (autocleared)	Bit: 0	RW

3.2.1.8 NTP Server Configuration Register

Configuration data of the NTP server.

Ntp ServerConfigMode Reg																											
Reg Description																											
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STRATUM								POLL_INTERVAL								PRECISION								-	BROADCAST	MULTICAST	UNICAST	-		IP_MODE	
RW								RW								RW								RO	RW	RW	RW	RO		RW	
Reset: 0x00000000																															
Offset: 0x0084																															

Name	Description	Bits	Access
STRATUM	Stratum Number	Bit:31:24	RW
POLL_INTERVAL	Poll Interval for Responses in Broadcast mode	Bit:23:15	RW
PRECISION	Precision of the clock	Bit:15:8	RW
-	Reserved, read 0	Bit:7	RO
BROADCAST	If the Server support Broadcasting time	Bit:6	RW
MULTICAST	If the Server support Multicast requests/responses	Bit:5	RW
UNICAST	If the Server support Unicast requests/responses	Bit:4	RW
-	Reserved, read 0	Bit:3:2	RO
IP_MODE	IPv4 = 1, IPv6 = 2, 0&3 are illegal	Bit:1:0	RW

3.2.1.9 NTP Server VLAN Configuration Registers

Enable/Disable and configure the VLAN tag at the NTP packets.

Ntp ServerConfigVlan Reg																													
Reg Description																													
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-															VLAN_EN	VLAN															
RO															RW	RW															
Reset: 0x00000000																															
Offset: 0x0088																															

Name	Description	Bits	Access
-	Reserved, read 0	Bit:31:17	RO
VLAN_EN	VLAN enable (0 disabled, 1 enabled)	Bit: 16	RW
VLAN	VLAN	Bit: 15:0	RW

3.2.1.10 NTP Server MAC1 Registers

MAC address of the node. LSB is transferred first on the network.

E.g. 0x01234567 => MAC: 67:45:32:01:XX:XX.

Ntp ServerConfigMac1 Reg																															
Reg Description																															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MAC(3)								MAC(2)								MAC(1)								MAC(0)							
RW								RW								RW								RW							
Reset: 0x00000000																															
Offset: 0x008C																															

Name	Description	Bits	Access
MAC(3)	MAC Byte 3	Bit:31:24	RW
MAC(2)	MAC Byte 2	Bit:23:16	RW
MAC(1)	MAC Byte 1	Bit:15:8	RW
MAC(0)	MAC Byte 0	Bit:7:0	RW

3.2.1.11NTP Server MAC2 Registers

MAC address of the node. LSB is transferred first on the network.

E.g. 0x0004567 => MAC: XX:XX:XX:67:45.

Ntp ServerConfigMac2 Reg																													
Reg Description																													
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
																MAC(5)								MAC(4)							
RO																RW								RW							
Reset: 0x00000000																															
Offset: 0x0090																															

Name	Description	Bits	Access
-	Reserved, read 0	Bit:31:16	RO
MAC(5)	MAC Byte 5	Bit:15:8	RW
MAC(4)	MAC Byte 4	Bit:7:0	RW

3.2.1.12NTP Server Config IP Registers

IP address of the NTP Server. Used as source IP. LSB is transferred first on the network. This is the full IP address for IPv4 and the highest part of IPv6.

Ntp ServerConfigIp Reg																													
Reg Description																													
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IP(3)								IP(2)								IP(1)								IP(0)							
RW								RW								RW								RW							
Reset: 0x00000000																															
Offset: 0x0094																															

Name	Description	Bits	Access
IP(3)	IP Byte 3 (Ipv4 and Ipv6)	Bit:31:24	RW
IP(2)	IP Byte 2 (Ipv4 and Ipv6)	Bit:23:16	RW
IP(1)	IP Byte 1 (Ipv4 and Ipv6)	Bit:15:8	RW
IP(0)	IP Byte 0 (Ipv4 and Ipv6)	Bit:7:0	RW

3.2.1.13NTP Server Config IP V6 1 Register

IPv6 address of the node. Used as source IP if in IPv6 mode, otherwise ignored. LSB is transferred first on the network.

Ntp ServerConfigIpv61 Reg																													
Reg Description																													
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IP(7)								IP(6)								IP(5)								IP(4)							
RW								RW								RW								RW							
Reset: 0x00000000																															
Offset: 0x0098																															

Name	Description	Bits	Access
IP(7)	IP Byte 7 (Ipv6 only)	Bit:31:24	RW
IP(6)	IP Byte 6 (Ipv6 only)	Bit:23:16	RW
IP(5)	IP Byte 5 (Ipv6 only)	Bit:15:8	RW
IP(4)	IP Byte 4 (Ipv6 only)	Bit:7:0	RW

3.2.1.14 NTP Server Config IP V6 2 Register

IPv6 address of the node. Used as source IP if in IPv6 mode, otherwise ignored. LSB is transferred first on the network.

Ntp ServerConfigIpv62 Reg																													
Reg Description																													
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IP(11)								IP(10)								IP(9)								IP(8)							
RW								RW								RW								RW							
Reset: 0x00000000																															
Offset: 0x009C																															

Name	Description	Bits	Access
IP(11)	IP Byte 11 (Ipv6 only)	Bit:31:24	RW
IP(10)	IP Byte 10 (Ipv6 only)	Bit:23:16	RW
IP(9)	IP Byte 9 (Ipv6 only)	Bit:15:8	RW
IP(8)	IP Byte 8 (Ipv6 only)	Bit:7:0	RW

3.2.1.15NTP Server Config IP V6 3 Register

IPv6 address of the node. Used as source IP if in IPv6 mode, otherwise ignored. LSB is transferred first on the network.

Ntp ServerConfigIpv63 Reg																													
Reg Description																													
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IP(15)								IP(14)								IP(13)								IP(12)							
RW								RW								RW								RW							
Reset: 0x00000000																															
Offset: 0x00A0																															

Name	Description	Bits	Access
IP(15)	IP Byte 15 (Ipv6 only)	Bit:31:24	RW
IP(14)	IP Byte 14 (Ipv6 only)	Bit:23:16	RW
IP(13)	IP Byte 13 (Ipv6 only)	Bit:15:8	RW
IP(12)	IP Byte 12 (Ipv6 only)	Bit:7:0	RW

3.2.1.16NTP Server Reference ID Register

NTP Reference ID in the NTP Frame

Ntp ServerReferenceId Reg																													
Reg Description																													
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REFERENCE_ID(0)								REFERENCE_ID(1)								REFERENCE_ID(2)								REFERENCE_ID(3)							
RW								RW								RW								RW							
Reset: 0x00000000																													
Offset: 0x00A4																													

Name	Description	Bits	Access
REFERENCE_ID(0-3)	NTP Reference ID as 4 byte ASCII text (left aligned an NULL(0) extended) one of these: LOCL: uncalibrated local clock CESM: calibrated Cesium clock RBDM: calibrated Rubidium clock PPS : calibrated quartz clock or other pulse-per-second source IRIG: Inter-Range Instrumentation Group ACTS: NIST telephone modem service USNO: USNO telephone modem service PTB : PTB (Germany) telephone modem service TDF : Allouis (France) Radio 164 kHz DCF : Mainflingen (Germany) Radio 77.5 kHz MSF : Rugby (UK) Radio 60 kHz WWV : Ft. Collins (US) Radio 2.5, 5, 10, 15, 20 MHz WWVB: Boulder (US) Radio 60 kHz WWVH: Kauai Hawaii (US) Radio 2.5, 5, 10, 15 MHz CHU : Ottawa (Canada) Radio 3330, 7335, 14670 kHz LORC: LORAN-C radionavigation system OMEG: OMEGA radionavigation system GPS : Global Positioning Service	Bit: 31:0	RW

3.2.1.17NTP Server UTC Information Control Register

Control Register for the UTC Information.

Ntp ServerUtcInfoControl Reg																													
Reg Description																													
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
READ_DONE	READ																													UTC_SMEARING_VAL	UTC_INFO_VAL
RO	RW	RO																												RW	RW
Reset: 0x00000000																															
Offset: 0x0100																															

Name	Description	Bits	Access
READ_DONE	UTC Info was read	Bit: 31	RO
READ	Read UTC Info (autocleared)	Bit: 30	RW
-	Reserved, read 0	Bit 29:2	RO
UTC_SMEARING_VAL	UTC Smearing mode valid (autocleared)	Bit 1	RW
UTC_INFO_VAL	UTC Info valid (autocleared)	Bit 0	RW

3.2.1.18NTP Server UTC Information Register

NTP UTC Information, depending on the ExtSync_Gen the UTC info can be set or is just read only. The only bit which is always settable (given that smearing is supported) is the UTC_LEAP_SMEARING bit

Ntp ServerUtcInfo Reg																													
Reg Description																													
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
UTC_OFFSET																-		UTC_OFFSET_VALID	LEAP59	LEAP61	LEAP59_IN_PROGRESS	LEAP61_IN_PROGRESS	UTC_LEAP_SMEARING	-							
RW																RO		RW	RW	RW	RO	RO	RW	RO							
Reset: 0x00000000																															
Offset: 0x0104																															

Name	Description	Bits	Access
UTC_OFFSET	UTC Offset	Bit: 31:16	RW
-	Reserved, read 0	Bit 15:14	RO
UTC_OFFSET_VALID	If UTC Offset is valid	Bit: 13	RW
LEAP59	Whether a Leap 59 will happen	Bit: 12	RW
LEAP61	Whether a Leap 61 will happen	Bit: 11	RW
LEAP59_IN_PROGRESS	Whether a Leap 59 is in progress (smearing)	Bit: 10	RO
LEAP61_IN_PROGRESS	Whether a Leap 61 is in progress(smearing)	Bit: 9	RO
UTC_LEAP_SMEARING	If UTC Leap second smearing shall be done	Bit: 8	RW

-	Reserved, read 0	Bit 7:0	RO

4 Design Description

The following chapters describe the internals of the NTP Server starting with the Top Level, which is a collection of subcores, followed by the description of all subcores.

4.1 Top Level – NTP Server

4.1.1 Parameters

The core must be parametrized at synthesis time. There are a couple of parameters which define the final behavior and resource usage of the core.

Name	Type	Size	Description
ResetBuffer_Gen	boolean	1	If the reset shall be synchronized to the System Clock in the core
ArpSupport_Gen	boolean	1	If the core shall support to response to ARP requests
IcmpSupport_Gen	boolean	1	If the core shall support to response to ICMP requests
UtcInitialUtcOffset_Gen	integer	1	Initial UTC offset value which is used
UtcLeapSmearing_Gen	boolean	1	If smearing for the UTC Leap Second handling is supported
UtcLeapSmearingRatePpb_Gen	natural	1	UTC Leap Second smearing rate in ns/60s
UnicastSupport_Gen	boolean	1	If the core shall support Unicast NTP
MulticastSupport_Gen	boolean	1	If the core shall support Multicast NTP
BroadcastSupport_Gen	boolean	1	If the core shall support Broadcast NTP
Layer3v4Support_Gen	boolean	1	If Ipv4 shall be supported
Layer3v6Support_Gen	boolean	1	If Ipv6 shall be supported
VlanSupport_Gen	boolean	1	Support for VLAN
PassThrough_Gen	boolean	1	If frames after the NTP shall be passed further

InternalLoopback_Gen	boolean	1	If loopback of the received packets to transmission shall be supported (possible only if PassThrough_Gen is disabled)
RedTagSupport_Gen	boolean	1	If the core shall support redundancy tag.
StaticConfig_Gen	boolean	1	If Static Configuration or AXI is used: true = Static, false = AXI
ExtSync_Gen	boolean	1	If external UTC information is used to sync: true = external, false = internal (register only)
ClockClkPeriodNanosecond_Gen	natural	1	Clock Period in Nanosecond: Default for 50 MHz = 20 ns
ClockClkPeriodFractNum_Gen	natural	1	Fractional Clock Period Numerator (0 if integer)
ClockClkPeriodFractDeNum_Gen	natural	1	Fractional Clock Period Denumerator (0 if integer)
RxDelayNanosecond10_Gen	integer	1	PHY receive delay (10Mbit)
RxDelayNanosecond100_Gen	integer	1	PHY receive delay (100Mbit)
RxDelayNanosecond1000_Gen	integer	1	PHY receive delay (1000Mbit)
TxDelayNanosecond10_Gen	integer	1	PHY transmit delay (10Mbit)
TxDelayNanosecond100_Gen	integer	1	PHY transmit delay (100Mbit)
TxDelayNanosecond1000_Gen	integer	1	PHY transmit delay (1000Mbit)
HighResSupport_Gen	boolean	1	If a high-resolution clock SysClkNx with alignment to SysClk is used
HighResFreqMultiply_Gen	natural	1	Multiplication factor of the high-resolution clock compared to SysClk
BufferSize_Gen	natural	1	Buffer size of the Frame

			Information FIFO
AxiAddressRangLow_Gen	std_logic_vector	32	AXI Base Address
AxiAddressRangeHigh_Gen	std_logic_vector	32	AXI Base Address plus Regis-terset Size Default plus 0xFFFF
Sim_Gen	boolean	1	If in Testbench simulation mode: true = Simulation, false = Synthesis

Table 5: Parameters

4.1.2 Structured Types

4.1.2.1 Clk_Time_Type

Defined in Clk_Package.vhd of library ClkLib
Type represents the time used everywhere. For this type overloaded operators + and – with different parameters exist.

Field Name	Type	Size	Description
Second	std_logic_vector	32	Seconds of time
Nanosecond	std_logic_vector	32	Nanoseconds of time
Fraction	std_logic_vector	2	Fraction numerator (mostly not used)
Sign	std_logic	1	Positive or negative time, 1 = negative, 0 = positive.
TimeJump	std_logic	1	Marks when the clock makes a time jump (mostly not used)

Table 6: Clk_Time_Type

4.1.2.2 Clk_UtcInfo_Type

Defined in Clk_Package.vhd of library ClkLib
Type represents the time used everywhere. For this type overloaded operators + and – with different parameters exist.

Field Name	Type	Size	Description
UtcOffset	std_logic_vector	15	UTC Offset in seconds
UtcOffsetValid	std_logic	1	UTC Offset is valid
Leap59	std_logic	1	Leap59 indication
Leap61	std_logic	1	Leap61 indication

Table 7: Clk_UtcInfo_Type

4.1.2.3 Ntp_ServerStaticConfig_Type

Defined in Ntp_ServerAddrPackage.vhd of library NtpLib
This is the type used for static configuration.

Field Name	Type	Size	Description
BroadcastModeEnable	std_logic	1	If Broadcast mode shall be used
MulticastModeEnable	std_logic	1	If Multicast mode shall be used
UnicastModeEnable	std_logic	1	If Unicast mode shall be used
Ipv4Enable	std_logic	1	If Ipv4 shall be used
Ipv6Enable	std_logic	1	If Ipv6 shall be used
Vlan	Ntp_Vlan_Type	1	The Pcp,Dei and Vid of the VLAN
VlanEnable	std_logic	1	If VLAN shall be used
Mac	Com-mon_Byte_Type	6	The source MAC to be used index 0 = MSB
Ip	Com-mon_Byte_Type	16	The source IP to be used, 4 bytes Ipv4, 16 bytes Ipv6, index 0 = MSB
Stratum	std_logic_vector	8	Stratum Number of the NTP Server
PollInterval	std_logic_vector	8	Poll Interval for Responses in Broadcast mode
Precision	std_logic_vector	8	Precision of the clock
ReferenceId	std_logic_vector	31	Reference ID in the NTP Frame
UtcLeapSmearing	std_logic	1	If UTC leap second smearing shall be done
UtcInfo	Clk_UtcInfo_Typ	1	The UTC information like

	e		offset, leap second etc.

Table 8: Ntp_ServerStaticConfig_Type

4.1.2.4 Ntp_ServerStaticConfigVal_Type

Defined in Ntp_ServerAddrPackage.vhd of library NtpLib
This is the type used for valid flags of the static configuration.

Field Name	Type	Size	Description
Enable_Val	std_logic	1	Enables the NTP Server
Mode_Val	std_logic	1	If the Mode shall be set
Vlan_Val	std_logic	1	If the VLAN shall be set
Mac_Val	std_logic	1	If the MAC shall be set
Ip_Val	std_logic	1	If the IP shall be set
ReferenceId_Val	std_logic	1	If the ReferenceId shall be set
UtcInfo_Val	std_logic	1	If UtcInfo shall be set

Table 9: Ntp_ServerStaticConfigVal_Type

4.1.2.5 Ntp_ServerStaticStatus_Type

Defined in Ntp_ServerAddrPackage.vhd of library NtpLib
This is the type used for static status supervision.

Field Name	Type	Size	Description
CoreInfo	Clk_CoreInfo_ Type	1	Infor about the Cores state
UtcInfo	Clk_UtcInfo_ Type	1	The UTC information like offset, leap second etc.
UtcLeap59InProgress	std_logic	1	Leap59 is in progress
UtcLeap61InProgress	std_logic	1	Leap61 is in progress

Table 10: Ntp_ServerStaticStatus_Type

4.1.2.6 Ntp_ServerStaticStatusVal_Type

Defined in Ntp_ServerAddrPackage.vhd of library NtpLib
This is the type used for valid flags of the static status supervision.

Field Name	Type	Size	Description
CoreInfo_Val	std_logic	1	Core Info valid
UtcInfo_Val	std_logic	1	UTC Info valid

Table 11: Ntp_ServerStaticStatusVal_Type

4.1.3 Entity Block Diagram

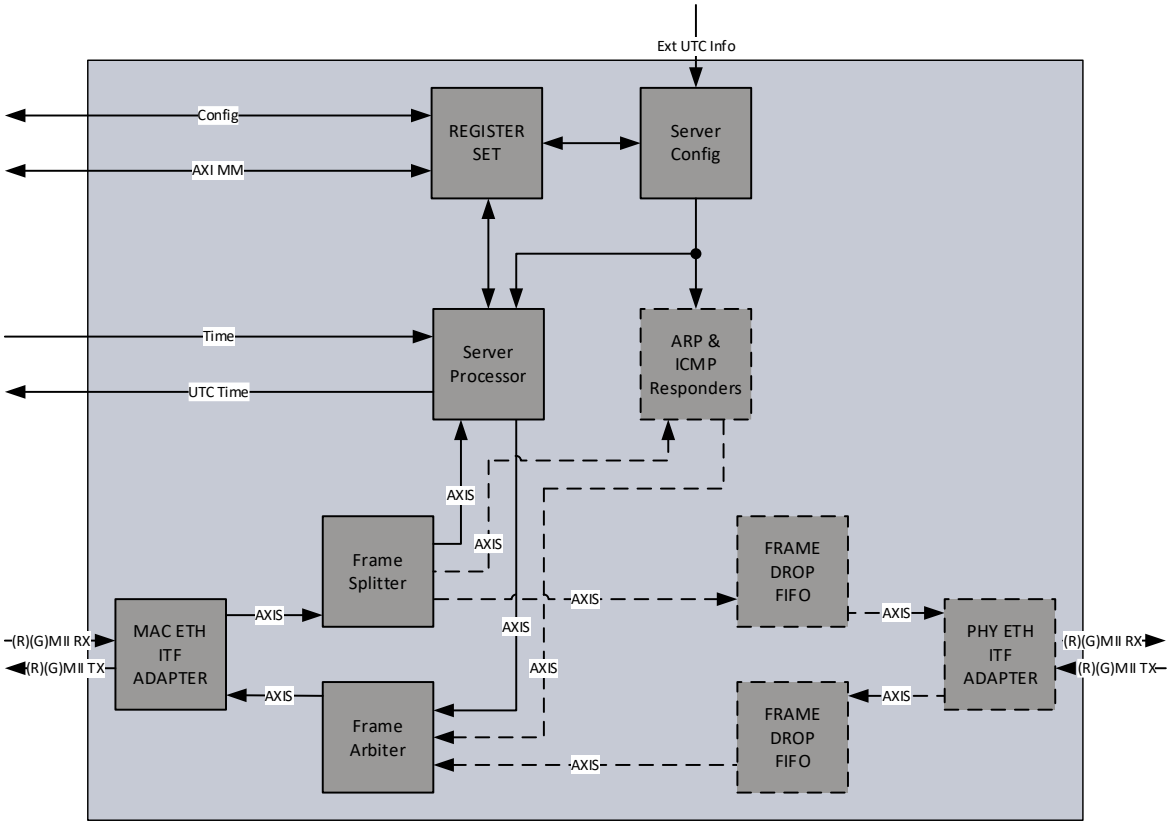

Figure 6: NTP Server

4.1.4 Entity Description

Frame Splitter

This module splits one AXI stream input to multiple AXI stream outputs, allowing the ARP Responder to receive ARP requests, forwarding frames through the core and forward frames to the server processor

Frame Arbiter

This modules multiplexes AXI stream inputs into one AXI stream output. Multiplexing is done on stream base, which means that once a stream has been started it will be the only stream forwarded until a TLAST is asserted, and then arbitration starts again. It handles two different priority levels. Each priority level is arbitrated in a round robin manner. Low priority streams can starve; high priority streams never starve.

Frame Drop Fifo

This module is AXI stream frame FIFO. It is always ready to receive data, so no throttling of the stream is necessary. It handles additionally a user drop-flag which allows explicitly dropping the current frame. In this design it is only used as store-and-forward FIFO, but with the drop-flag. The FIFO on the RX path allows to drop NTP and corrupted frames (they shall not be forwarded). The FIFO on the TX path buffers the incoming data stream for the case when an internal frame is processed (send a NTP or ARP response). The FIFO in the loopback path also allows to drop NTP and corrupted frames.
The FIFOs are optional either for the through put mode or for an internal loopback.

Server Processor

This block is the heart the NTP Server. The Server Processor timestamps the incoming frames, extracts the information of the NTP request and stores this information in a frame information FIFO. With the data from this FIFO the frame creator generates the response which includes the transmit timestamp. Depending on the selected mode also the NTP broadcast frames are generated by the Server Processor. Additionally, UTC handling is done by the Server Processor block.
See 4.2.1 for more details.

Server Config

This block controls the configuration of the server. There are multiple sources possible, like the configuration via the register set, static configuration from externally or also UTC information from externally.
See 4.2.2 for more details.

ARP & ICMP Responders

These modules answers ARP/ICMP requests with ARP/ICMP responses. This module is optional.
See 4.2.3 for more details.

MAC & PHY Ethernet Interface Adapter

This module converts the Media Independent Interface (MII) to AXI stream and vice versa. In parallel it has a SFD detector for each path which generates an event when a SFD is detected; this is used for timestamping in the RX/TX Processors. It is also in charge of generating correct Interframe Gaps and a Preamble with SFD.
See 4.2.4 for more details.

Registerset

This module is an AXI4Lite Memory Mapped Slave. It allows to configure the NTP Server. It can be configured to either run in AXI or StaticConfig mode. If in StaticConfig mode, the configuration of the Server is done via signals and can be easily done from within the FPGA without CPU. If in AXI mode, a AXI Master has to configure the Server with AXI writes to the registers, which is typically done by a CPU See 4.2.5 for more details.

4.1.5 Entity Declaration

Name	Dir	Type	Size	Description
Generics				
General				
ResetBuffer_Gen	-	boolean	1	If the reset shall be synchronized to the System Clock in the core
ArpSupport_Gen	-	boolean	1	If the core shall support to response to ARP requests
IcmpSupport_Gen	-	boolean	1	If the core shall support to response to ICMP requests
UtcInitialUtcOffset_Gen	-	integer	1	Initial UTC offset value which is used
UtcLeapSmearing_Gen	-	boolean	1	If smearing for the UTC Leap Second handling is supported
UtcLeapSmearingRatePpb_Gen	-	natural	1	UTC Leap Second smearing rate in ns/s (ppb)
UnicastSupport_Gen	-	boolean	1	If the core shall support Unicast NTP
MulticastSupport_Gen	-	boolean	1	If the core shall support Multicast

				NTP
BroadcastSup-port_Gen	-	boolean	1	If the core shall support Broadcast NTP
Lay-er3v4Support_Gen	-	boolean	1	If Ipv4 shall be supported
Lay-er3v6Support_Gen	-	boolean	1	If Ipv6 shall be supported
VlanSupport_Gen	-	boolean	1	Support for VLAN
PassThrough_Gen	-	boolean	1	If frames shall be passed through the core
RedTagSupport_Gen	-	boolean	1	If the core shall support redundancy tag.
StaticConfig_Gen	-	boolean	1	If Static Configura-tion or AXI is used: true = Static, false = AXI
ExtSync_Gen	-	boolean	1	If external UTC information is used to sync: true = external, false = internal (register only)
ClockClkPeriodNano-second_Gen	-	natural	1	Clock Period in Nanosecond: Default for 50 MHz = 20 ns
ClockClkPeriodFract-Num_Gen	-	natural	1	Fractional Clock Period Numerator (0 if integer)
ClockClkPeriod-FractDeNum_Gen	-	natural	1	Fractional Clock Period Denumerator (0 if integer)
RxDelayNanosec-ond10_Gen	-	integer	1	PHY receive delay (10Mbit)
RxDelayNanosec-	-	integer	1	PHY receive delay

ond100_Gen				(100Mbit)
RxDelayNanosec-ond1000_Gen	-	integer	1	PHY receive delay (1000Mbit)
TxDelayNanosec-ond10_Gen	-	integer	1	PHY transmit delay (10Mbit)
TxDelayNanosec-ond100_Gen	-	integer	1	PHY transmit delay (100Mbit)
TxDelayNanosec-ond1000_Gen	-	integer	1	PHY transmit delay (1000Mbit)
HighResSupport_Gen	-	boolean	1	If a high-resolution clock SysClkNx with alignment to SysClk is used
HighResFreqMulti-ply_Gen	-	natural	1	Multiplication factor of the high-resolution clock compared to SysClk
BufferSize_Gen	-	natural	1	Buffer size of the Frame Information FIFO
AxiAddressRang Low_Gen	-	std_logic_vector	32	AXI Base Address
AxiAddressRange High_Gen	-	std_logic_vector	32	AXI Base Address plus Registerset Size Default plus 0xFFFF
Sim_Gen	-	boolean	1	If in Testbench simulation mode: true = Simulation, false = Synthesis
Ports				
System				
SysClk_ClkIn	in	std_logic	1	System Clock
SysClkNx_ClkIn	in	std_logic	1	High-resolution clock (multiple of Sys Clock)
SysRstN_RstIn	in	std_logic	1	System Reset
Config				

StaticConfig_DatIn	in	Ntp_Server StaticConfig_Type	1	Static Configuration
StaticConfig_ValIn	in	Ntp_Server StaticConfigVal _Type	1	Static Configuration valid
Status				
StaticStatus_DatOut	out	Ntp_Server StaticStatus_Type	1	Static Status
StaticStatus_ValOut	out	Ntp_Server StaticStatusVal _Type	1	Static Status valid
Timer				
Timer1ms_EvtIn	in	std_logic	1	Adjusted Clock aligned 1 millisecond Timer event
Time Input				
ClockTime_DatIn	in	Clk_Time_Type	1	Adjusted Clock Time
ClockTime_ValIn	in	std_logic	1	Adjusted Clock Time valid
(R)(G)Mii RX Clk/Rst Input				
(R)(G)MiiRxClk_ClkIn	in	std_logic	1	RX Clock
(R)(G)MiiRxRstN_RstIn	in	std_logic	1	Reset aligned with RX Clock
(R)(G)Mii TX Clk/Rst Input				
(R)(G)MiiTxClk_ClkIn	in	std_logic	1	TX Clock
(R)(G)MiiTxRstN_RstIn	in	std_logic	1	Reset aligned with TX Clock
(R)(G)Mii RX Data Input/Output				
(R)(G)MiiRxDv_Ena	in/ out	std_logic	1	RX Data valid
(R)(G)MiiRxErr_Ena	in/ out	std_logic	1	RX Error
(R)(G)MiiRxData_Dat	in/ out	std_logic_vector	2-8	RX Data MII:4, RMII:2, GMII:8, RGMII:4
(R)(G)MiiCol_Dat	in/ out	std_logic	1	Collision
(R)(G)MiiCrs_Dat	in/	std_logic	1	Carrier Sense

	out			
(R)(G)Mii TX Data Input/Output				
(R)(G)MiiTxEn_Ena	in/ out	std_logic	1	TX Data valid
(R)(G)MiiTxErr_Ena	in/ out	std_logic	1	TX Error
(R)(G)MiiTxData_Dat	in/ out	std_logic_vector	2-8	TX Data MII:4, RMII:2, GMII:8, RGMII:4
External UTC Info Input				
UtcInfoExtSync_DatIn	in	Clk_UtcInfo_Type	1	UTC information input from external
UtcInfoExtSync_ValIn	in	std_logic	1	UTC information input valid from external
UTC Time Output				
UtcTime_DatOut	out	Clk_Time_Type	1	UTC Time output
UtcTime_ValOut	out	std_logic	1	UTC Time output valid
AXI4 Lite Slave				
AxiWriteAddrValid _ValIn	in	std_logic	1	Write Address Valid
AxiWriteAddrReady _RdyOut	out	std_logic	1	Write Address Ready
AxiWriteAddrAddress _AdrIn	in	std_logic_vector	32	Write Address
AxiWriteAddrProt _DatIn	in	std_logic_vector	3	Write Address Protocol
AxiWriteDataValid _ValIn	in	std_logic	1	Write Data Valid
AxiWriteDataReady _RdyOut	out	std_logic	1	Write Data Ready
AxiWriteDataData _DatIn	in	std_logic_vector	32	Write Data
AxiWriteDataStrobe _DatIn	in	std_logic_vector	4	Write Data Strobe
AxiWriteRespValid _ValOut	out	std_logic	1	Write Response Valid
AxiWriteRespReady _RdyIn	in	std_logic	1	Write Response Ready
AxiWriteResp Response_DatOut	out	std_logic_vector	2	Write Response
AxiReadAddrValid _ValIn	in	std_logic	1	Read Address Valid

AxiReadAddrReady_RdyOut	out	std_logic	1	Read Address Ready
AxiReadAddrAddress_AdrIn	in	std_logic_vector	32	Read Address
AxiReadAddrProt_DatIn	in	std_logic_vector	3	Read Address Protocol
AxiReadDataValid_ValOut	out	std_logic	1	Read Data Valid
AxiReadDataReady_RdyIn	in	std_logic	1	Read Data Ready
AxiReadData Response_DatOut	out	std_logic_vector	2	Read Data
AxiReadDataData_DatOut	out	std_logic_vector	32	Read Data Re-sponse

Table 12: NTP Server

4.2 Design Parts

The NTP server core consists of a couple of subcores. Each of the subcores itself consist again of smaller function block. The following chapters describe these subcores and their functionality.

4.2.1 Server Processor

4.2.1.1 Entity Block Diagram

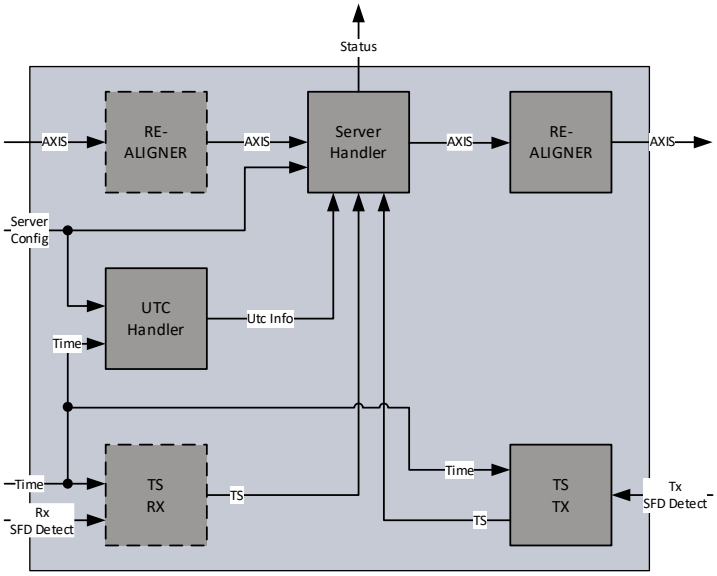

Figure 7: Server Processor

4.2.1.2 Entity Description

RX Timestamper

This module takes a snapshot of the UTC time when the SFD detected event was asserted by the Interface Adapter. The timestamp is buffered and aligned with the incoming frame. The RX timestamper not instantiated if only broadcast mode supported.

TX Timestamper

This module takes a snapshot of the UTC time when the SFD detected event was asserted by the Interface Adapter. The timestamp is buffered and aligned with the outgoing frame.

Server Handler

This module extracts the information of the NTP request and stores this information in a frame information FIFO. With the data from this FIFO the frame creator generates the response which includes the transmit timestamp. Depending on the selected mode also the NTP broadcast frames are generated by the Server Handler.

UTC Handler

This module handles based on the time (TAI) from the Counter Clock the UTC Offset and the leap seconds. Additionally, smearing of the leap second is done by the UTC handler once enabled.

Re-Aligner

This module allows aligning the AXI Data stream as required. The input can be 32/24/16/8 bit aligned and the output can also be 32/24/16/8 bit aligned. From an external input, the output alignment can be requested. This is used for alignment of the NTP start to a 32 bit boundary (Some mappings cause that the header is not 32 bit aligned anymore) again, and for realignment to a constant 32bit wide stream again.

4.2.1.3 Entity Declaration

Name	Dir	Type	Size	Description
Generics				
General				
ClockClkPeriodNanosecond_Gen	-	natural	1	Clock Period in Nanosecond: Default for 50 MHz = 20 ns
RxDelayNanosecond10_Gen	-	integer	1	PHY receive delay (10Mbit)
RxDelayNanosecond100_Gen	-	integer	1	PHY receive delay (100Mbit)
RxDelayNanosecond1000_Gen	-	integer	1	PHY receive delay (1000Mbit)
TxDelayNanosecond10_Gen	-	integer	1	PHY transmit delay (10Mbit)

TxDelayNanosec-ond100_Gen	-	integer	1	PHY transmit delay (100Mbit)
TxDelayNanosec-ond1000_Gen	-	integer	1	PHY transmit delay (1000Mbit)
HighResSupport_Gen	-	boolean	1	If a high-resolution clock SysClkNx with alignment to SysClk is used
HighResFreqMulti-ply_Gen	-	natural	1	Multiplication factor of the high-resolution clock compared to SysClk
UtcInitialUtcOff-set_Gen	-	integer	1	Initial UTC offset value which is used
UtcLeapSmear-ing_Gen	-	boolean	1	If smearing for the UTC Leap Second handling is support-ed
UtcLeapSmear-ingRatePpb_Gen	-	natural	1	UTC Leap Second smearing rate in ns/60s
UnicastSupport_Gen	-	boolean	1	If the core shall support Unicast NTP
MulticastSupport_Gen	-	boolean	1	If the core shall support Multicast NTP
BroadcastSup-port_Gen	-	boolean	1	If the core shall support Broadcast NTP
Lay-er3v4Support_Gen	-	boolean	1	If Ipv4 shall be supported
Lay-er3v6Support_Gen	-	boolean	1	If Ipv6 shall be supported
VlanSupport_Gen	-	boolean	1	Support for VLAN
RedTagSupport_Gen	-	boolean	1	If the core shall support redundancy tag.

BufferSize_Gen	-	natural	1	Buffer size of the Frame Information FIFO
Sim_Gen	-	boolean	1	If in Testbench simulation mode: true = Simulation, false = Synthesis
Ports				
System				
SysClk_ClkIn	in	std_logic	1	System Clock
SysClkNx_ClkIn	in	std _logic	1	High resolution Timestamping Clock
SysRstN_RstIn	in	std_logic	1	System Reset
Enable Input				
Enable_EnaIn	in	std_logic	1	Core Enabled
Time Input				
ClockTime_DatIn	in	Clk_Time_Type	1	Adjusted Clock Time
ClockTime_ValIn	in	std_logic	1	Adjusted Clock Time valid
Timer				
Timer1ms_EvtIn	in	std_logic	1	Adjusted Clock aligned 1 millisecond Timer event
UTC Time				
UtcTime_DatOut	out	Clk_Time_Type	1	UTC Time
UtcTime_ValOut	out	std_logic	1	UTC Time valid
Link Speed Input				
LinkSpeed_DatIn	in	Common_ LinkSpeed_Type	1	Link Speed of the interface
Frame Input				
SfdDetectedRx_EvtIn	in	std_logic	1	Start of RX Frame Delimiter detected
Axi Input				
AxisValid_ValIn	in	std_logic	1	AXI Stream frame input
AxisReady_ValIn	in	std_logic	1	
AxisData_DatIn	in	std_logic_vector	32	
AxisStrobe_ValIn	in	std_logic_vector	4	
AxisKeep_ValIn	in	std_logic_vector	4	
AxisLast_ValIn	in	std_logic	1	

AxisUser_DatIn	in	std_logic_vector	3	
Drop Output				
Drop_ValOut	out	std_logic	1	If frame shall be dropped
Frame Output				
SfdDetectedTx_EvtIn	in	std_logic	1	Start of TX Frame Delimiter detected
Axi Output				
AxisValid_ValOut	out	std_logic	1	AXI Stream frame output
AxisReady_ValIn	in	std_logic	1	
AxisData_DatOut	out	std_logic_vector	32	
AxisStrobe_ValOut	out	std_logic_vector	4	
AxisKeep_ValOut	out	std_logic_vector	4	
AxisLast_ValOut	out	std_logic	1	
AxisUser_DatOut	out	std_logic_vector	3	
Selcted Input				
Selected_DatIn	in	std_logic	1	Select input from the frame Arbiter
Server Config Output				
ServerConfig_DatOut	out	Ntp_ServerConfig_Type	1	NTP Server configuration
ServerConfig_ValOut	out	std_logic	1	NTP Server configuration valid
Server Config Input				
ServerConfig_DatIn	in	Ntp_ServerConfig_Type	1	NTP Server configuration

Table 13: Server Processor

4.2.2 Server Config

4.2.2.1 Entity Block Diagram

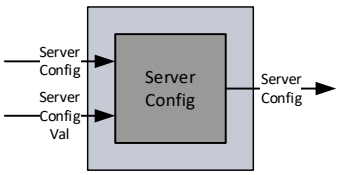

Figure 8: Server Config

4.2.2.2 Entity Description

Server Config

This module controls the configuration of the server. It checks if a configuration is supported and it stores the configured parameter once it is valid.

4.2.2.3 Entity Declaration

Name	Dir	Type	Size	Description
Generics				
General				
UtcInitialUtcOffset_Gen	-	integer	1	Initial UTC offset value which is used
UtcLeapSmearing_Gen	-	boolean	1	If smearing for the UTC Leap Second handling is supported
UnicastSupport_Gen	-	boolean	1	If the core shall support Unicast NTP
MulticastSupport_Gen	-	boolean	1	If the core shall support Multicast NTP
BroadcastSupport_Gen	-	boolean	1	If the core shall support Broadcast NTP
Layer3v4Support_Gen	-	boolean	1	If Ipv4 shall be supported
Layer3v6Support_Gen	-	boolean	1	If Ipv6 shall be supported
VlanSupport_Gen	-	boolean	1	Support for VLAN
ExtSync_Gen	-	boolean	1	If external UTC information is used to sync: true = external, false = internal (register only)
Ports				
System				

SysClk_ClkIn	in	std_logic	1	System Clock
SysClkNx_ClkIn	in	std _logic	1	High resolution Timestamping Clock
SysRstN_RstIn	in	std_logic	1	System Reset
Server Configuration Input				
ServerConfig_DatIn	in	Ntp_ServerConfig_Type	1	NTP Server Configuration
ServerConfig_ValIn	in	Ntp_ServerConfigVal_Type	1	NTP Server Configuration valid
Server Configuration Output				
ServerConfig_DatOut	in	Ntp_ServerConfig_Type	1	Stored NTP Server Configuration

Table 14: Server Configuration

4.2.3 ARP & ICMP Responders

4.2.3.1 Entity Block Diagram

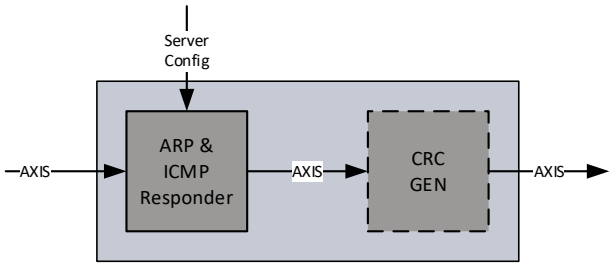

Figure 9: ARP Responder

4.2.3.2 Entity Description

ARP/ICMP Responder

These modules receives the ARP or ICMP requests and answer with a corresponding ARP or ICMP response to it. The ARP/ICMP responder gets its configuration like MAC address and IP from the Server Config.
These are two individual blocks

CRC GEN

This module generates the CRC of the ARP response.

4.2.3.3 Entity Declaration

Name	Dir	Type	Size	Description
Generics				
General				
NoCrc_Gen	-	boolean	1	No CRC generation
Ports				
System				
SysClk_ClkIn	in	std_logic	1	System Clock
SysRstN_RstIn	in	std_logic	1	System Reset
Enable Input				
Enable_EnaIn	in	std_logic	1	Module enable
Server Config Input				
LocalMAC_DatIn	in	Common_Byte_Type	6	The MAC address of the NTP client
LocalIpv4_DatIn	in	Common_Byte_Type	4	The IPv4 address of the NTP Client, index 0 = MSB
LocalIpv6_DatIn	in	Common_Byte_Type	16	The IPv6 address of the NTP Client, index 0 = MSB
Timer				
Timer1ms_EvtIn	in	std_logic	1	Adjusted Clock aligned 1 millisecond Timer event
Axi Input				
AxisValid_ValIn	in	std_logic	1	AXI Stream frame input
AxisReady_ValIn	in	std_logic	1	
AxisData_DatIn	in	std_logic_vector	32	
AxisStrobe_ValIn	in	std_logic_vector	4	
AxisKeep_ValIn	in	std_logic_vector	4	
AxisLast_ValIn	in	std_logic	1	
AxisUser_DatIn	in	std_logic_vector	3	
Axi Output				
AxisValid_ValOut	out	std_logic	1	AXI Stream frame output
AxisReady_ValIn	in	std_logic	1	
AxisData_DatOut	out	std_logic_vector	32	
AxisStrobe_ValOut	out	std_logic_vector	4	
AxisKeep_ValOut	out	std_logic_vector	4	

AxisLast_ValOut	out	std_logic	1
AxisUser_DatOut	out	std_logic_vector	3

Table 15: ARP Responder

4.2.4 Ethernet Interface Adapter

4.2.4.1 Entity Block Diagram

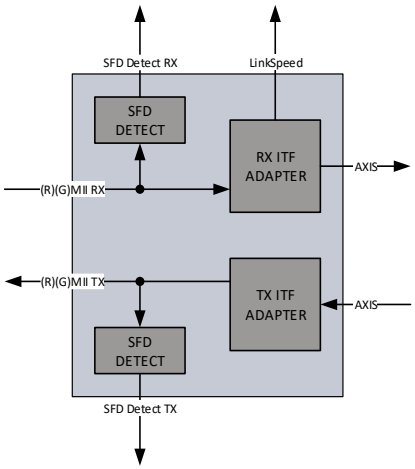

Figure 10: Ethernet Interface Adapter

4.2.4.2 Entity Description

SFD Detector

This module detects the Start of Frame Delimiter (SFD) on the (R)(G)MII stream. It runs directly on the (R)(G)MII clock domain for minimal jitter on the timestamp point detection. Once the SFD is detected, an event is signaled which is used by the timestamper.

RX Interface Adapter

This module convert the Media Independent Interface (R)(G)MII data stream (2/4/8bit) into a 32bit AXI stream. First bytes on the cable are mapped to the AXI MSB of the data array. It contains an asynchronous FIFO to on one hand do clock domain crossing from the external clock to the system clock and on the other hand also to minimal buffer data for speed differences. The FIFO size is kept quite small to assure correct timestamp alignment with the frame. It converts the different data widths into a 32bit block AXI stream. The Preamble and SFD are removed on reception. Also, it detects the link speed based on the interface clock.

TX Interface Adapter

This module convert the 32bit AXI stream into a Media Independent Interface (R)(G)MII data stream (2/4/8bit) which is continuous. The MSB of the AXI data array is mapped to the first byte on the cable. It contains an asynchronous FIFO to

on one hand do clock domain crossing from the system clock to the external clock and on the other hand also to minimal buffer data for speed differences. The Fifo size is kept quite small to assure correct timestamp alignment with the frame. It converts the 32bit block AXI stream into the different data widths. The Preamble and SFD are added before transmission. It also assures the correct interframe gap between frames.

4.2.4.3 Entity Declaration

Name	Dir	Type	Size	Description
Generics				
Interface Adapter				
ClockClkPeriodNano-second_Gen	-	natural	1	Integer Clock Period
IoFf_Gen	-	boolean	1	Shall IO flip flops be instantiated
Ports				
System				
SysClk_ClkIn	in	std_logic	1	System Clock
SysRstN_RstIn	in	std_logic	1	System Reset
(R)(G)Mii RX Clk/Rst Input				
(R)(G)MiiRxClk_ClkIn	in	std_logic	1	RX Clock
(R)(G)MiiRxRstN_RstIn	in	std_logic	1	Reset aligned with RX Clock
(R)(G)Mii TX Clk/Rst Input				
(R)(G)MiiTxClk_ClkIn	in	std_logic	1	TX Clock
(R)(G)MiiTxRstN_RstIn	in	std_logic	1	Reset aligned with TX Clock
(R)(G)Mii RX Data Input/Output				
(R)(G)MiiRxDv_Ena	In/ out	std_logic	1	RX Data valid
(R)(G)MiiRxErr_Ena	In/ out	std_logic	1	RX Error
(R)(G)MiiRxData_Dat	In/ out	std_logic_vector	2-8	RX Data MII:4, RMII:2, GMII:8, RGMII:4
(R)(G)MiiCol_Dat	In/ out	std_logic	1	Collision

(R)(G)MiiCrs_Dat	In/ out	std_logic	1	Carrier Sense
(R)(G)Mii TX Data Input				
(R)(G)MiiTxEn_Ena	In/ out	std_logic	1	TX Data valid
(R)(G)MiiTxErr_Ena	In/ out	std_logic	1	TX Error
(R)(G)MiiTxData_Dat	In/ out	std_logic_vector	2-8	TX Data MII:4, RMII:2, GMII:8, RGMII:4
Link Speed Output				
LinkSpeed_DatOut	out	Common_ LinkSpeed_Type	1	Link Speed of the interface
SfdDetected Output				
(R)(G)MiiInSfdDetected_EvtOut	out	std_logic	1	Start of Frame Delimiter detected
(R)(G)MiiOutSfdDetected_EvtOut	out	std_logic	1	Start of Frame Delimiter detected
Axi Input				
AxisValid_ValIn	in	std_logic	1	AXI Stream frame input
AxisReady_ValOut	out	std_logic	1	
AxisData_DatIn	in	std_logic_vector	32	
AxisStrobe_ValIn	in	std_logic_vector	4	
AxisKeep_ValIn	in	std_logic_vector	4	
AxisLast_ValIn	in	std_logic	1	
AxisUser_DatIn	in	std_logic_vector	3	
Axi Output				
AxisValid_ValOut	out	std_logic	1	AXI Stream frame output
AxisReady_ValIn	in	std_logic	1	
AxisData_DatOut	out	std_logic_vector	32	
AxisStrobe_ValOut	out	std_logic_vector	4	
AxisKeep_ValOut	out	std_logic_vector	4	
AxisLast_ValOut	out	std_logic	1	
AxisUser_DatOut	out	std_logic_vector	3	

Table 16: Ethernet Interface Adapter

4.2.5 Registerset

4.2.5.1 Entity Block Diagram

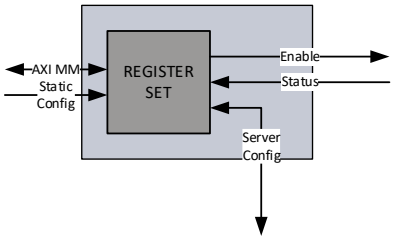

Figure 11: Registerset

4.2.5.2 Entity Description

Register Set

This module is an AXI4Lite Memory Mapped Slave. It provides access to the server status and allows configuring the NTP Server. AXI4Lite only supports 32 bit wide data access, no byte enables, no burst, no simultaneous read and writes and no unaligned access. It can be configured to either run in AXI or StaticConfig mode. If in StaticConfig mode, the configuration of the Server is done via signals and can be easily done from within the FPGA without CPU. For each parameter a valid signal is available, the enable signal shall be set last (or simultaneously). To change parameters the NTP Server has to be disabled and enabled again. If in AXI mode, a AXI Master has to set the configuration with AXI writes to the registers, which is typically done by a CPU. Parameters can in this case also be changed at runtime.

4.2.5.3 Entity Declaration

Name	Dir	Type	Size	Description
Generics				
General				
UtcInitialUtcOffset_Gen	-	integer	1	Initial UTC offset value which is used
UtcLeapSmearing_Gen	-	boolean	1	If smearing for the UTC Leap Second handling is supported
UnicastSupport_Gen	-	boolean	1	If the core shall

				support Unicast NTP
MulticastSupport_Gen	-	boolean	1	If the core shall support Multicast NTP
BroadcastSup-port_Gen	-	boolean	1	If the core shall support Broadcast NTP
Lay-er3v4Support_Gen	-	boolean	1	If Ipv4 shall be supported
Lay-er3v6Support_Gen	-	boolean	1	If Ipv6 shall be supported
VlanSupport_Gen	-	boolean	1	Support for VLAN
ExtSync_Gen	-	boolean	1	If external UTC information is used to sync: true = external, false = inter-nal (register only)
Register Set				
StaticConfig_Gen	-	boolean	1	If Static Configura-tion or AXI is used
AxiAddressRange Low_Gen	-	std_logic_vector	32	AXI Base Address
AxiAddressRange High_Gen	-	std_logic_vector	32	AXI Base Address plus Registerset Size
Ports				
System				
SysClk_ClkIn	in	std_logic	1	System Clock
SysRstN_RstIn	in	std_logic	1	System Reset
Config				
StaticConfig_DatIn	in	Ntp_Server StaticConfig_Type	1	Static Configuration
StaticConfig_ValIn	in	Ntp_Server StaticConfigVal _Type	1	Static Configuration valid
Status				
StaticStatus_DatOut	out	Ntp_Server	1	Static Status

		StaticStatus_Type		
StaticStatus_ValOut	out	Ntp_Server StaticStatusVal _Type	1	Static Status valid
AXI4 Lite Slave				
AxiWriteAddrValid _ValIn	in	std_logic	1	Write Address Valid
AxiWriteAddrReady _RdyOut	out	std_logic	1	Write Address Ready
AxiWriteAddrAddress _AdrIn	in	std_logic_vector	32	Write Address
AxiWriteAddrProt _DatIn	in	std_logic_vector	3	Write Address Protocol
AxiWriteDataValid _ValIn	in	std_logic	1	Write Data Valid
AxiWriteDataReady _RdyOut	out	std_logic	1	Write Data Ready
AxiWriteDataData _DatIn	in	std_logic_vector	32	Write Data
AxiWriteDataStrobe _DatIn	in	std_logic_vector	4	Write Data Strobe
AxiWriteRespValid _ValOut	out	std_logic	1	Write Response Valid
AxiWriteRespReady _RdyIn	in	std_logic	1	Write Response Ready
AxiWriteResp Response_DatOut	out	std_logic_vector	2	Write Response
AxiReadAddrValid _ValIn	in	std_logic	1	Read Address Valid
AxiReadAddrReady _RdyOut	out	std_logic	1	Read Address Ready
AxiReadAddrAddress _AdrIn	in	std_logic_vector	32	Read Address
AxiReadAddrProt _DatIn	in	std_logic_vector	3	Read Address Protocol
AxiReadDataValid _ValOut	out	std_logic	1	Read Data Valid
AxiReadDataReady _RdyIn	in	std_logic	1	Read Data Ready
AxiReadData Response_DatOut	out	std_logic_vector	2	Read Data
AxiReadDataData _DatOut	out	std_logic_vector	32	Read Data Re-sponse
Error Input				
Ntp_ErrIn	in	std_logic	1	An error happened
Status Input				

RequestReceived_ValIn	in	std_logic	1	
ResponseSent_ValIn	in	std_logic	1	
RequestDropped_ValIn	in	std_logic	1	
BroadcastSent_ValIn	in	std_logic	1	
UtcLeap59InProgress_ValIn	in	std_logic	1	
UtcLeap61InProgress_ValIn	in	std_logic	1	
Config Output				
ServerConfig_DatOut	out	Ntp_ServerConfig_Type	1	NTP Server Configuration data output
ServerConfig_ValOut	out	Ntp_ServerConfigVal_Type	1	NTP Server Configuration valid output
Enable Output				
NtpServerEnable_DatOut	out	std_logic	1	Enable NTP Sever

Table 17: Registerset

4.3 Configuration example

4.3.1 Static Configuration

```
constant NtpStaticConfig_Con : Ntp_ServerStaticConfig_Type := (
    BroadcastModeEnable                             => '0',
    MulticastModeEnable                             => '0',
    UnicastModeEnable                               => '1',
    Ipv4Enable                                      => '1',
    Ipv6Enable                                      => '0',
    Vlan                                            => Ntp_Vlan_Type_Rst_Con,
    VlanEnable                                      => '1',
    MAC                                             => (
        0                                           => x"4E",
        1                                           => x"54",
        2                                           => x"4C",
        3                                           => x"10",
        4                                           => x"00",
        5                                           => x"00"),
    Ip                                              => (
        0                                           => x"C0",
        1                                           => x"A8",
        2                                           => x"00",
        3                                           => x"10",
        others                                      => x"00"),
    Stratum                                         => x"01",
    PollInterval                                    => x"04",
    Precision                                       => x"E3",
    ReferenceId                                     => x"4C4F434C", -- LOCL
    UtcLeapSmearing                                 => '0',
    UtcInfo                                         => Clk_UtcInfo_Type_Rst_Con,
);

constant NtpStaticConfigVal_Con : Ntp_ServerStaticConfigVal_Type := (
    Enable_Val                                      => '1',
    Mode_Val                                        => '1',
    Vlan_Val                                        => '1',
    Mac_Val                                         => '1',
    Ip_Val                                          => '1',
    ReferenceId_Val                                 => '1',
    UtcInfo_Val                                     => '1'
);
```

4.3.2 AXI Configuration

The following code is a simplified pseudocode from the testbench: The base address of the NTP Server is 0x10000000.

```
-- NTP
-- Config Server
-- Stratum 1, Poll Interval 4, Precision 227, Unicast/Multicast/Broadcast mode, IPv4
AXI WRITE 10000084,0x0104E371

-- VLAN 0x4000 (unused)
AXI WRITE 10000088,0x00004000

-- Mac: 00:01:02:03:04:05
AXI WRITE 1000008C,0x03020100
AXI WRITE 10000090,0x00000504

-- IP: 192.168.7.1
AXI WRITE 10000094,0x0107A8C0

-- Reference Id LOCL
AXI WRITE 100000A4,0x4C4F434C

-- Set Config valid bits
AXI WRITE 10000080,0x0000001F

-- set UTC Offset 37, valid, no leap, no smearing
AXI WRITE 10000104,0x00252000
-- set UTC Info and smearing valid
AXI WRITE 10000100,0x00000003

-- enable NTP Server
AXI WRITE 10000000,0x00000001
```

4.4 Clocking and Reset Concept

4.4.1 Clocking

To keep the design as robust and simple as possible, the whole NTP Server including the Counter Clock and all other cores from NetTimeLogic are run in one clock domain. This is considered to be the system clock. Per Default this clock is 50MHz. Where possible also the interfaces are run synchronous to this clock. For clock domain crossing asynchronous Fifos with gray counters or message patterns with meta-stability flip-flops are used. Clock domain crossings for the AXI interface is moved from the AXI slave to the AXI interconnect.
To increase the timestamping resolution for some very small logic parts a high resolution clock is used. This clock is optional and it must be a multiple of the System Clock.

Clock	Frequency	Description
System		
System Clock	50MHz (Default)	System clock where the NTP Server runs on as well as the counter clock etc.
High Resolution Clock	250 MHz (Default)	Optional High-resolution clock (multiple of Sys Clock)
(R)(G)MII Interface		
PHY (R)(G)MII RX Clock	2.5/25/125MHz	Asynchronous, external receive clock from the PHY also used for the MAC. Depending on the interface not all frequencies apply.
PHY (R)(G)MII TX Clock	2.5/25/125MHz	Asynchronous, external transmit clock to/from the PHY also used for the MAC. Depending on the interface not all frequencies apply.
AXI Interface		
AXI Clock	50MHz (Default)	Internal AXI bus clock, same as the system clock

Table 18: Clocks

4.4.2Reset

In connection with the clocks, there is a reset signal for each clock domain. All resets are active low. All resets can be asynchronously set and shall be synchronously released with the corresponding clock domain. All resets shall be asserted

for the first couple (around 8) clock cycles. All resets shall be set simultaneously and released simultaneously to avoid overflow conditions in the core. See the reference designs top file for an example of how the reset shall be handled.

Reset	Polarity	Description
System		
System Reset	Active low	Asynchronous set, synchronous release with the system clock
(R)(G)MII Interface		
PHY (R)(G)MII RX Reset	Active low	Asynchronous set, synchronous release with the (R)(G)MII RX clock
PHY (R)(G)MII TX Reset	Active low	Asynchronous set, synchronous release with the (R)(G)MII TX clock
AXI Interface		
AXI Reset	Active low	Asynchronous set, synchronous release with the AXI clock, which is the same as the system clock

Table 19: Resets

5 Resource Usage

Since the FPGA Architecture between vendors and FPGA families differ there is a split up into the two major FPGA vendors.

5.1 Intel/Altera (Cyclone 10)

Configuration	FFs	LUTs	BRAMs	DSPs
Minimal (Only Unicast, ARP Support, No leap second smearing, No VLAN and No RedTag support)	3747	9503	36	16
Maximal (Unicast, Multicast, Broadcast, ARP Support, leap second smearing, VLAN and RedTag support)	4057	10876	46	16

Table 20: Resource Usage Intel/Altera

5.2 AMD/Xilinx (Artix 7)

Configuration	FFs	LUTs	BRAMs	DSPs
Minimal (Only Unicast, ARP Support, No leap second smearing, No VLAN and No RedTag support)	3746	6292	8	8
Maximal (Unicast, Multicast, Broadcast, ARP Support, leap second smearing, VLAN and RedTag support)	4227	7148	8	8

Table 21: Resource Usage AMD/Xilinx

6 Delivery Structure

```
AXI                                 -- AXI library folder
 |-Library                          -- AXI library component sources
 |-Package                          -- AXI library package sources

CLK                                 -- CLK library folder
 |-Library                          -- CLK library component sources
 |-Package                          -- CLK library package sources

COMMON                              -- COMMON library folder
 |-Library                          -- COMMON library component sources
 |-Package                          -- COMMON library package sources

NTP                                 -- NTP library folder
|-Core                              -- NTP library cores
 |-Doc                              -- NTP library cores documentations
 |-Library                          -- NTP library component sources
 |-Package                          -- NTP library package sources
 |-Refdesign                        -- NTP library cores reference designs
 |-Testbench                        -- NTP library cores testbench sources and sim/log

SIM                                 -- SIM library folder
 |-Doc                              -- SIM library command documentation
 |-Package                          -- SIM library package sources
 |-Testbench                        -- SIM library testbench template sources
 |-Tools                            -- SIM simulation tools
```

7 Testbench

The NTP Server testbench consist of 4 parse/port types: AXI, CLK, ETH and NTP. Multiple instances exist. NTP0 CLK, NTP1 CLK, NTP0 NTP, NTP1 NTP and MAC0 ETH ports are all multiplexed with the MAC0 ETH MUX to one Ethernet channel connected to the port going to the PHY from the DUT (which acts like a MAC). PHY0 is connected to the port going to the MAC from the DUT (which acts like a PHY)

The NTP Client ports take the CLK ports times as reference and sets the timestamps aligned with the time from the CLK ports. The NTP Client ports are sending NTP Request and take the time of the Clock instance as reference and checks it with the times in the frames from the DUT. In addition, for configuration and result checks an AXI read and write port is used in the testbench and for accessing more than one AXI slave also an AXI interconnect is required.

With this Setup multiple NTP client can be simulated.

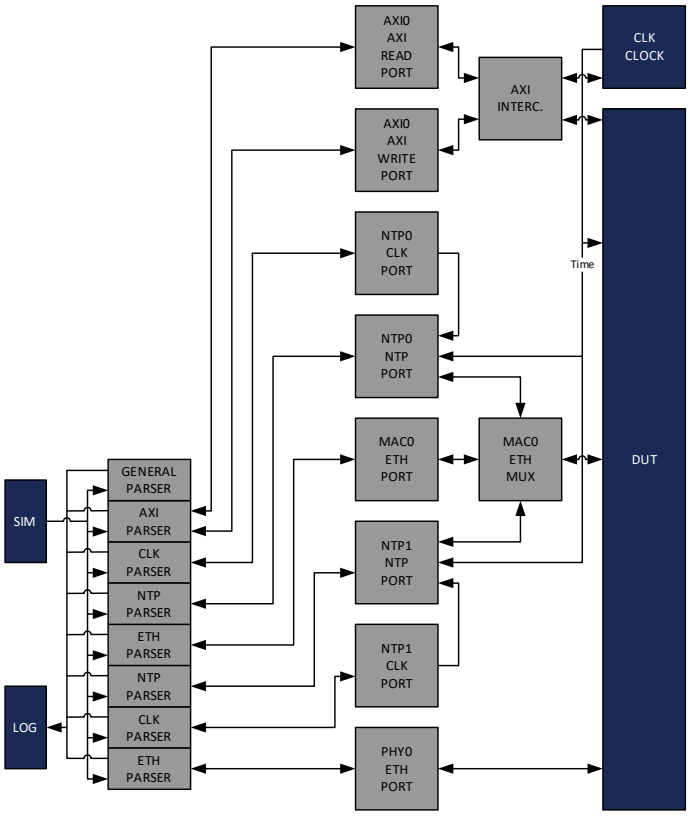

Figure 12: Testbench Framework

For more information on the testbench framework check the Sim_ReferenceManual documentation.

With the Sim parameter set the time base for timeouts are divided by 1000 to 100000 to speed up simulation time.

7.1 Run Testbench

1. Run the general script first

```
source XXX/SIM/Tools/source_with_args.tcl
```

2. Start the testbench with all test cases

```
src XXX/NTP/Testbench/Core/NtpServer/Script/run_Ntp_ServerMii_Tb.tcl
```

3. Check the log files LogFileX.txt in the XXX/NTP/Testbench/Core/NtpServer/Log/ folder for simulation results.

8 Reference Designs

The NTP Server design contains a PLL to generate all necessary clocks (cores are run at 50 MHz), an instance of the NTP Server IP core and an instance of the Adjustable Counter Clock IP core (needs to be purchased separately). The Reference Design is intended to be connected to any NTP Client. The Reference Design is using MII in 100Mbit full duplex as Ethernet link. If a second Ethernet Port is available on the FPGA board pass through can be enabled.
All generics can be adapted to the specific needs.

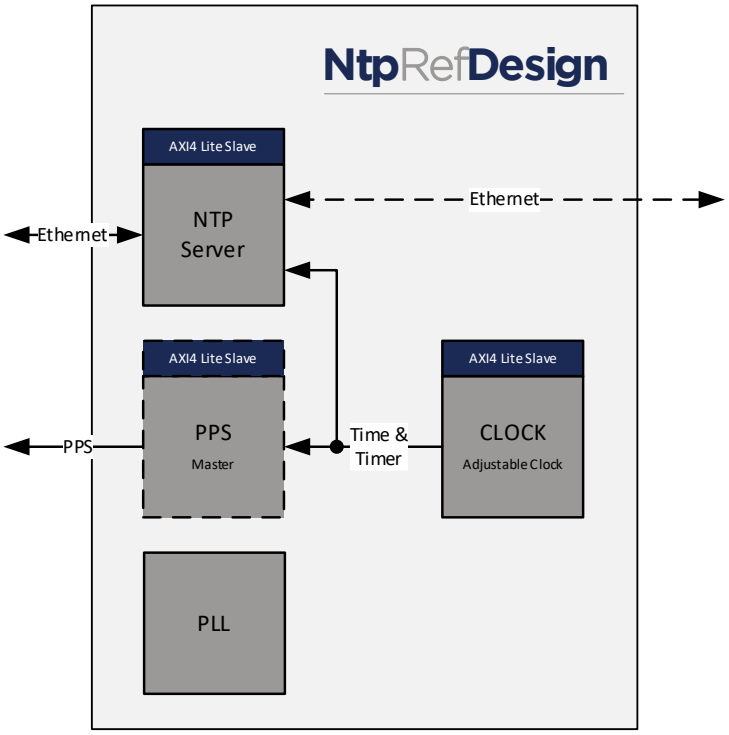

Figure 13: Reference Design

8.1 Intel/Altera: Cyclone 10 LP RefKit

The Cyclone 10 LP RefKit board is an FPGA board from Trenz Electronic. with a Cyclone 10 FPGA from Intel/Altera. (https://shop.trenz-electronic.de/de/TEI0009-02-055-8CA-Cyclone-10-LP-RefKit-10CL055-Development-Board-32-MByte-SDRAM-16-MByte-Flash).

1. Open Quartus 18.1
2. Open Project
   /NTP/Refdesign/Altera/C10LpRefKit/NtpServerMii/NtpServerMii.qpf

3. If the optional core PPS Master Clock is available add the files from the corresponding folders (PPS/Core, PPS/Library and PPS/Package)
4. Change the generics (PpsMasterAvailable_Gen) in Quartus (in the settings menu, not in VHDL) to true for the optional cores that are available.
5. Rerun implementation
6. Download to FPGA via JTAG

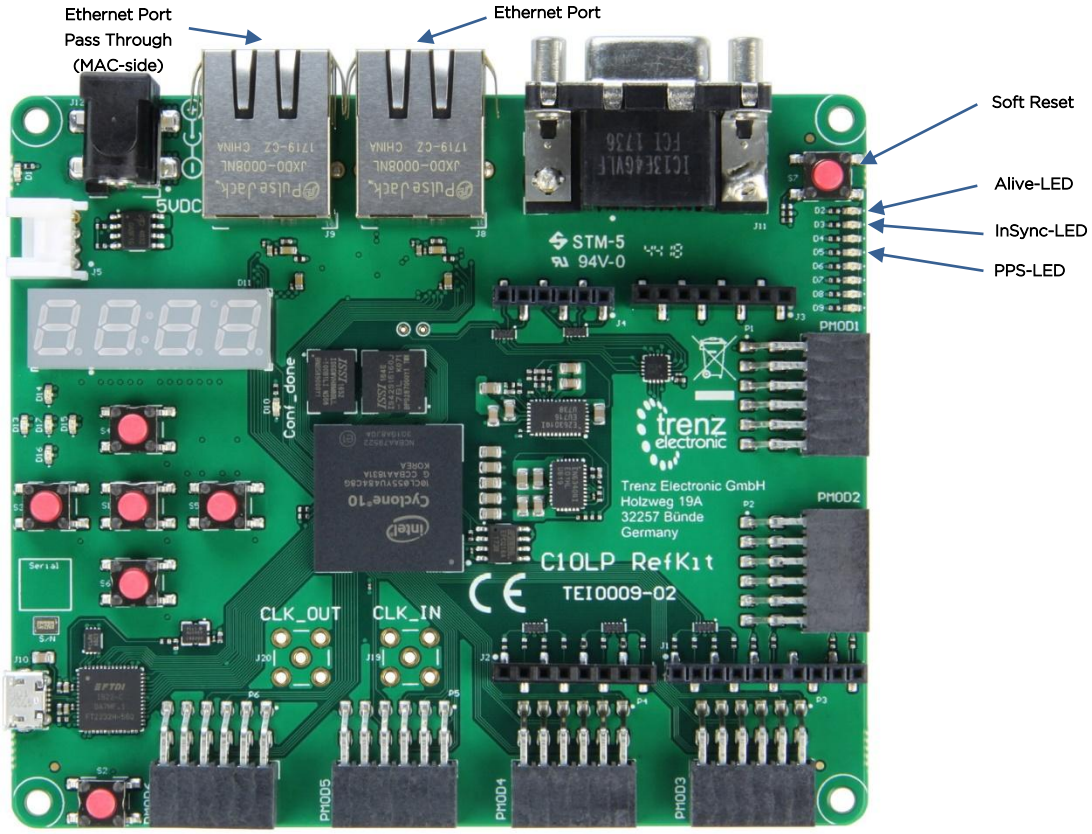

Figure 14: Cyclone 10 LP RefKit (source Trenz Electronic)

8.2 AMD/Xilinx: Digilent Arty

The Arty board is an FPGA board from Digilent Inc. with an Artix7 FPGA from AMD/Xilinx. (http://store.digilentinc.com/arty-board-artix-7-fpga-development-board-for-makers-and-hobbyists/)

1. Open Vivado 2019.1
   Note: If a different Vivado version is used, see chapter 8.3.
2. Run TCL script /NTP/Refdesign/Xilinx/Arty/NtpServerMii/NtpServerMii.tcl
   a. This has to be run only the first time and will create a new Vivado Project
3. If the project has been created before open the project and do not rerun the project TCL

4. If the optional core PPS Master Clock is available add the files from the corresponding folders (PPS/Core, PPS/Library and PPS/Package) to the corresponding Library (PpsLib).
5. Change the generics (PpsMasterAvailable_Gen) in Vivado (in the settings menu, not in VHDL) to true for the optional cores that are available.
6. Rerun implementation
7. Download to FPGA via JTAG

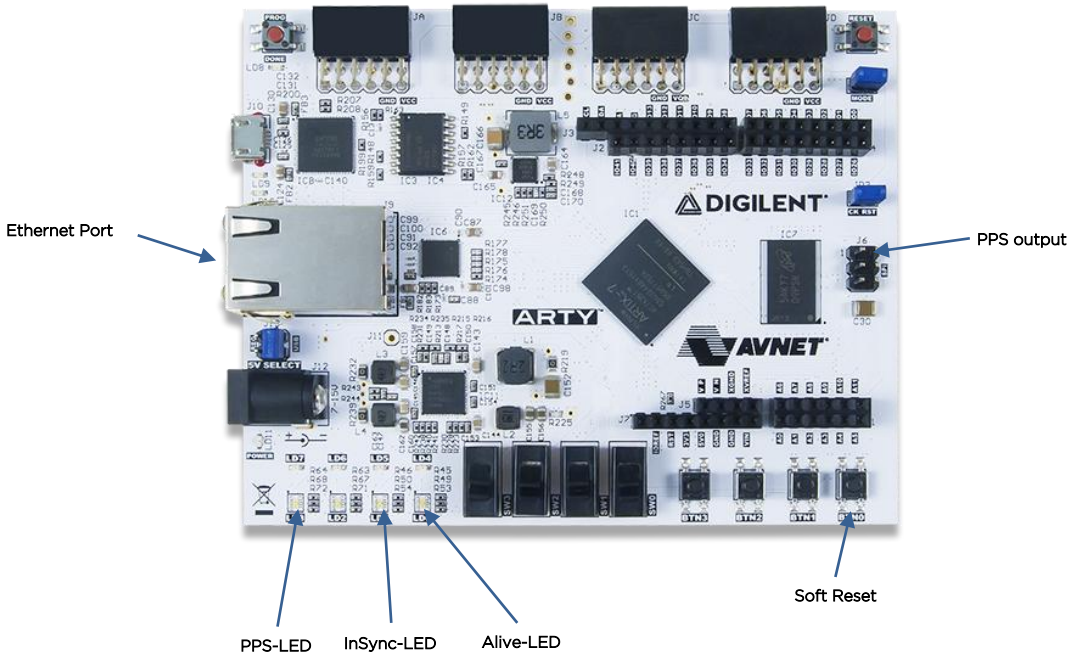

Figure 15: Arty (source Digilent Inc)

8.3 AMD/Xilinx: Vivado version

The provided TCL script for creation of the reference-design project is targeting AMD/Xilinx Vivado 2019.1.

If a lower Vivado version is used, it is recommended to upgrade to Vivado 2019.1 or higher.

If a higher Vivado version is used, the following steps are recommended:

- Before executing the project creation TCL script, the script's references of Vivado 2019 should be manually replaced to the current Vivado version. For example, if version Vivado 2022 is used, then:
  - The statement occurrences:

    ```
    set_property flow "Vivado Synthesis 2019" $obj
    ```

    shall be replaced by:

```
set_property flow "Vivado Synthesis 2022 $obj
```

- The statement occurrences:

```
set_property flow "Vivado Implementation 2019" $obj
```

shall be replaced by:

```
set_property flow "Vivado Implementation 2022" $obj
```

- After executing the project creation TCL script, the AMD/Xilinx IP cores, such as the Clocking Wizard core, might be locked and a version upgrade might be required. To do so:
  1. At "Reports" menu, select "Report IP Status".
  2. At the opened "IP Status" window, select "Upgrade Selected". The tool will upgrade the version of the selected IP cores.

A List of tables

B List of figures