AIONYX

Datasheet

MainBoard

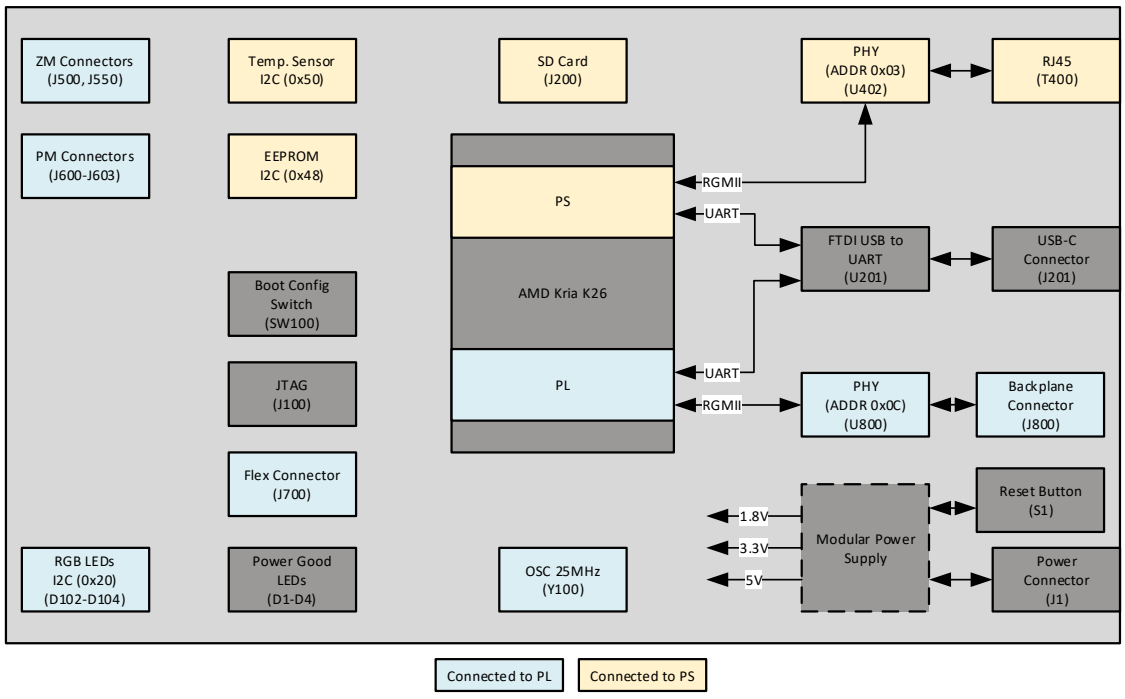
The AIONYX MainBoard serves as a carrier board for the AMD KRIA K26 SoM, equipped with 4x A53 and 2x R5 ARM CPUs, alongside an FPGA. It interconnects the power supply, Pmod™ and Zmod™ compatible interfaces, and includes a 10/100/1000Mbit PHY connected to the CPU. It features USB/UART ports for CPU and FPGA connectivity, as well as an SD card slot for booting. Additionally, back-plane and Flex connectors are available for further expansions.

Key Features

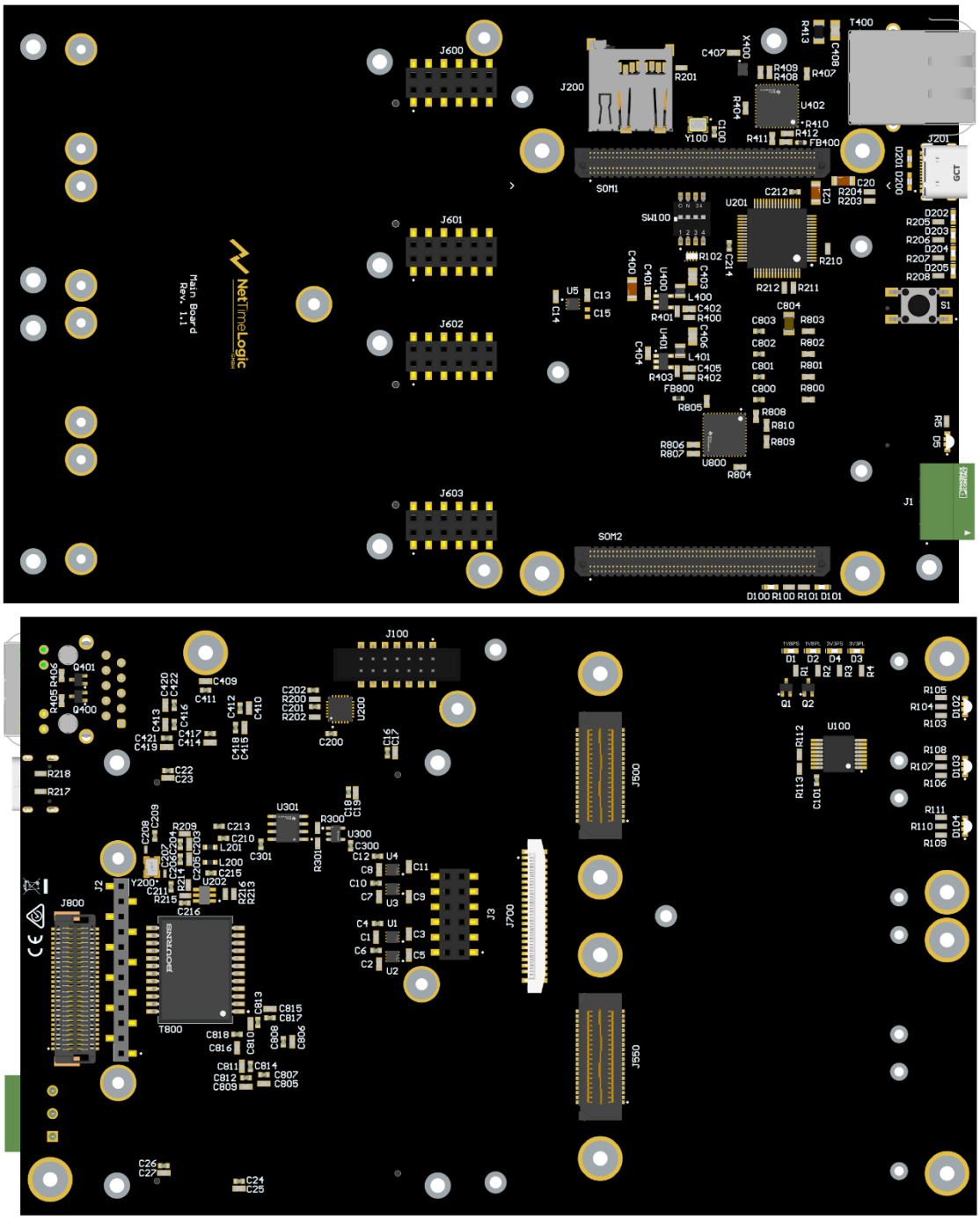
- 2x ZM Module Slots (Zmod™ compatible)
- 4x PM Module Slots (Pmod™ compatible)
- USB-C Dual UART for PS and PL
- 10/100/1000Mbit PHY connected to PS MAC
- Power Supply as a Module
- Flex Connector and Backplane Connector connected to the PL

Main Board

Block Diagram



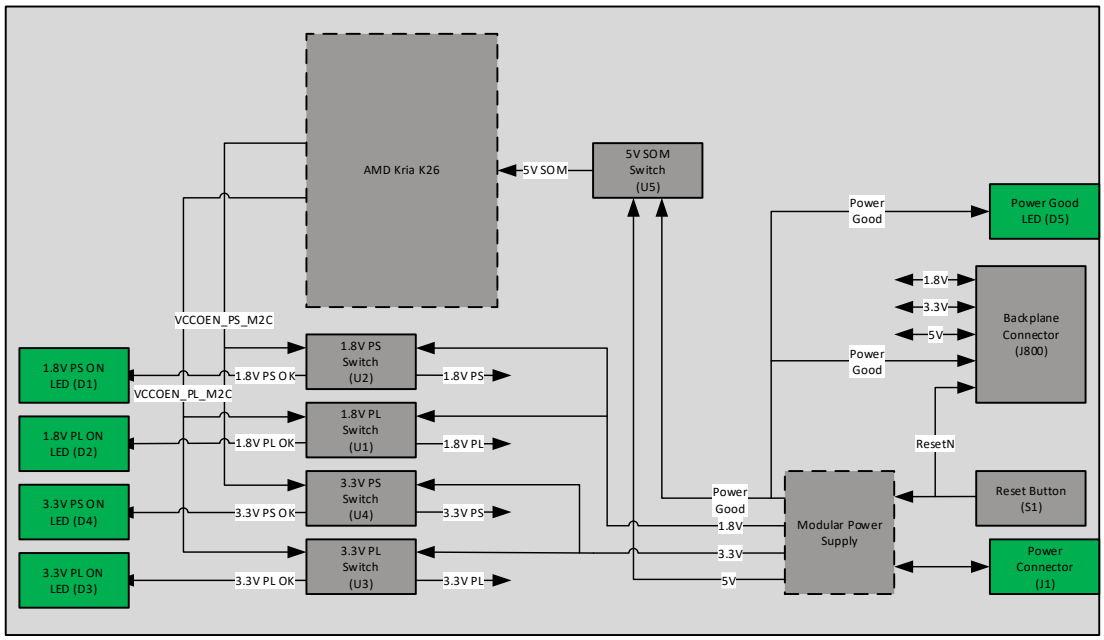
Module Overview



Board size 160x100mm

Carrier Board Power Concept

The standalone carrier board is powered via the Power Connector J1. The supported voltage range is provided by the Modular Power Supply (typically 9-36 VDC). The voltages generated by the Modular Power Supply are also supplied to the Backplane Connector. If there is a Power Supply on the Backplane, the 1.8V, 3.3V, 5V and Power Good Indication must be provided via connector J800.

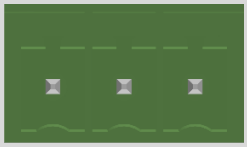


Signals	
ResetN	The reset can be done manually via the Reset Button S1 or remotely via the Backplane. When activated, it disables the power supplies on the module. It is an active low reset.
Power Good	Power Good indicates that the voltage from the Modular Power Supply is available. If the board is powered via the Backplane, the signal must be provided from there. Power Good is visualized on the Power Good LED (D5)
5V	5V power plane from the Power Supply.
3.3V	3.3V power plane from the Power Supply.
1.8V	1.8V power plane from the Power Supply.
5V SOM	5V SOM is switched on by the Power Good indication.
VCCOEN_PS_M2C	After the 5V SOM is enabled, the K26 SOM asserts the VCCOEN_PS_M2C signal, indicating to the carrier card to turn on the supply rails for the PS peripheral devices.
VCCOEN_PL_M2C	After the 5V SOM is enabled, the K26 SOM asserts the VCCOEN_PL_M2C signal, indicating to the carrier card to turn on the supply rails for the PL peripheral devices, as well as all VCCO rails for the HPIO and HDIO banks.
3.3V PS	3.3V PS is switched on by the VCCOEN_PS_M2C signal from the K26.
3.3V PL	3.3V PL is switched on by the VCCOEN_PL_M2C signal from the K26.
1.8V PS	1.8V PS is switched on by the VCCOEN_PS_M2C signal from the K26.
1.8V PL	1.8V PL is switched on by the VCCOEN_PL_M2C signal from the K26.
3.3V PS OK	If the 3.3V PS is available, it is indicated on the 3.3V PS LED (D4).
3.3V PL OK	If the 3.3V PL is available, it is indicated on the 3.3V PL LED (D3).
1.8V PS OK	If the 1.8V PS is available, it is indicated on the 1.8V PS LED (D1).
1.8V PL OK	If the 1.8V PL is available, it is indicated on the 1.8V PL LED (D2).

Bank Voltages	
501 (PS MIO)	Fixed 1.8V supplied by the K26 SOM
502 (PS MIO)	Fixed 1.8V supplied by the K26 SOM
43 (HDB HDIO)	3.3V PL
44 (HDC HDIO)	3.3V PL
45 (HDA HDIO)	3.3V PL
64 (HPC HPIO)	1.8V PL
65 (HPB HPIO)	1.8V PL
66 (HPA HPIO)	1.8V PL

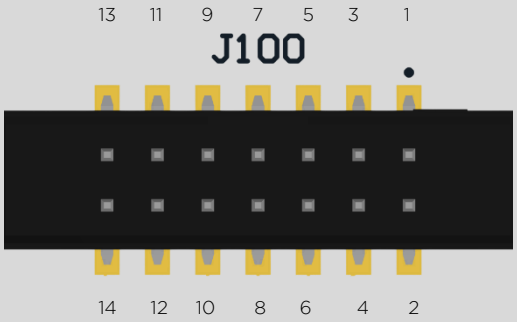
Connector Overview and Pin Description

Power Connector (J1)	
Type	1803280 (PHOENIX CONTACT)
Counterpart	1851054 (PHOENIX CONTACT)
Information	The supported voltages depend on the modular power supply. Before connect check first what the power supply does support!



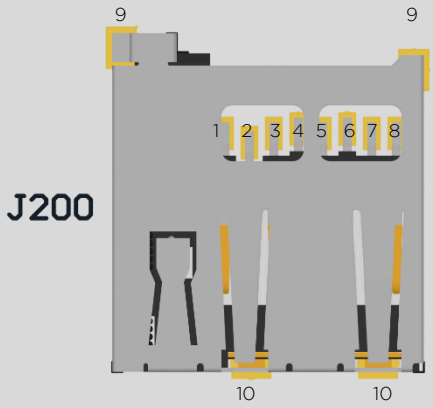
Pin	Signal	I/O	Description
1	VCC EXT	I	VCC from external power supply (voltage range must match with the power supply module)
2	GND EXT	I	Ground of the external power supply
3	SHIELD	I	Shield/Earth

JTAG (J100)	
Type	2BHR-14-VUA-SMT (Adam Tech)
Counterpart	14-pin 2mm pitch JTAG Connector with ribbon cable



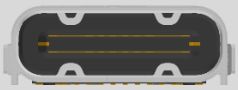
Pin	Signal	I/O	Description	Kria K26 Package Pin (Bank | SOM Connector Pin)
1	GND	I	Ground	-
2	VREF	O	Target Reference Voltage 1.8 V PS	-
3	GND	I	Ground	-
4	JTAG TMS	I	JTAG Test Mode Select	**N21** (Bank 503 | SOM 1 A22)
5	GND	I	Ground	-
6	JTAG TCK	I	JTAG Test Clock	**R19** (Bank 503 | SOM 1 A25)
7	GND	I	Ground	-
8	JTAG TDO	O	JTAG Test Data Out	**T21** (Bank 503 | SOM 1 A23)
9	GND	I	Ground	-
10	JTAG TDI	I	JTAG Test Data In	**R18** (Bank 503 | SOM 1 A24)
11	GND	I	Ground	-
12	NC	-	Not Connected	-
13	GND	I	Ground	-
14	JTAG HALT	I	JTAG Halt (PS_SRST_B)	**N19** (Bank 503 | SOM 1 C16)

SD CARD (J200)	
Type	693071010811 (Würth Micro SD Card Connector)
Information	The SD Card slot is powered with 3.3V but connected on a 1.8V Bank. Therefore, a TI TXS02612 level shifter performs the required translation.



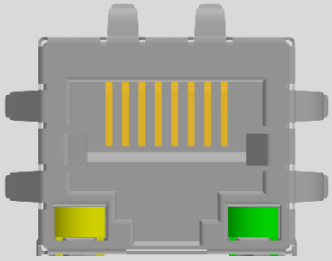
Pin	Signal	I/O	Description	Kria K26 Package Pin (Bank | SOM Connector Pin)
1	SD DAT2	I	Data[2]	**J21** (PS_MIO48 | Bank 501 | SOM 1 C35)
2	SD DAT3	O	Data[3]	**M18** (PS_MIO49 | Bank 501 | SOM 1 C36)
3	SD CMD	I	Command	**M19** (PS_MIO50 | Bank 501 | SOM 1 B36)
4	VDD	I	3.3V PS Powered	-
5	SD CLK	I	Clock	**L21** (PS_MIO51 | Bank 501 | SOM 1 B37)
6	GND	I	Ground	-
7	SD DAT0	I	Data[0]	**L20** (PS_MIO46 | Bank 501 | SOM 1 D34)
8	SD DAT1	O	Data[1]	**H21** (PS_MIO47 | Bank 501 | SOM 1 C34)
9	SD CD	I	Card Detect Indication	**K20** (PS_MIO45 | Bank 501 | SOM 1 D33)
10	GND (GND)	I	Ground of the CD loop	-

USB-C/UART (J201)	
Type	USB4105-GF-A (GCT USB Type C, 2.0 Connector)
Counterpart	USB-C Cable
Information	The USB Type C connector provides two UART interfaces via a FTDI USB to UART chip (U200 FT2232HL). One goes to the PS and the other to the PL.



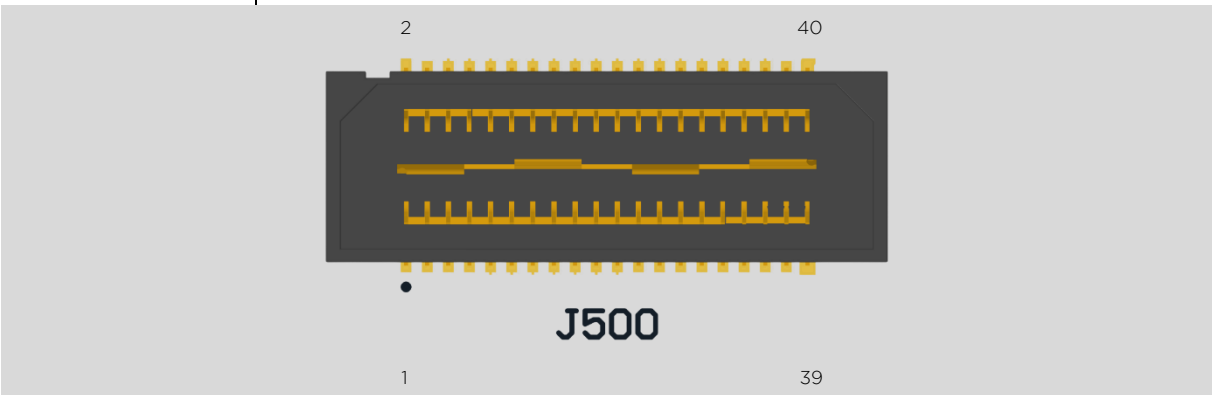
Pin	Signal	I/O	Description	Kria K26 Package Pin (Bank | SOM Connector Pin)
-	UART 1 TXD	I	UART TX Line to the PL	**K13** (Bank 45 | SOM 1 B17)
-	UART 1 RXD	O	UART RX Line from the PL	**K12** (Bank 45 |SOM 1 B18)
-	UART 2 TXD	I	UART TX Line to the PS	**D20** (PS_MIO74 | Bank 502 | SOM 1 A43)
-	UART 2 RXD	O	UART RX Line from the PS	**A19** (PS_MIO75 | Bank 502 | SOM 1 A44)

Ethernet PS (T400)	
Type	JXD0-0015NL (Pulse RJ45 Connector with internal magnetics)
Counterpart	RJ45 Ethernet Cable
Information	The RJ45 connector is connected via TI 10/100/1000 Mbit/s PHY (U402 DP83869HM) to the PS of the Kria. The Green LED is connected to the LED0 Pin of the PHY and the Yellow LED is connected to the LED2 of the PHY. Green (default): 10/100M/1G Link-up Yellow (default): TX and RX Activity The PHY has the SMI Address 0x03.



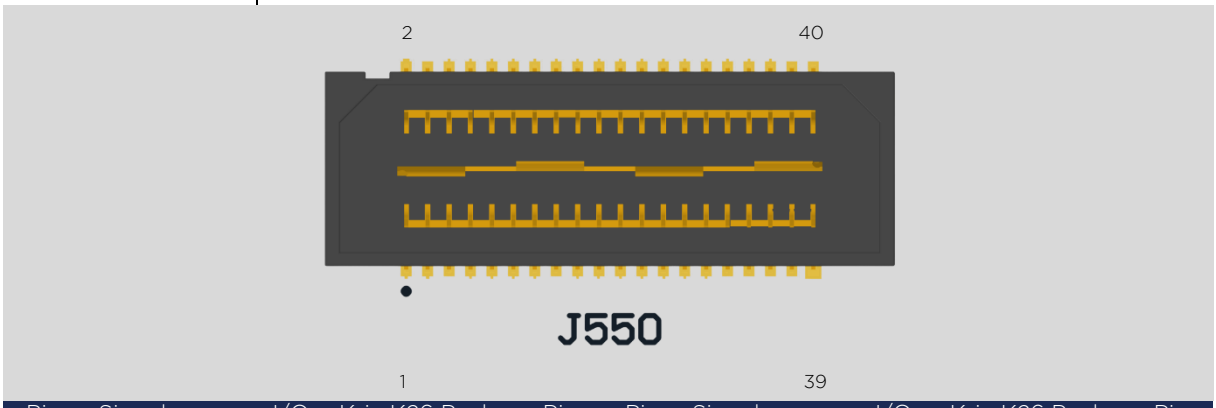
Pin	Signal	I/O	Description	Kria K26 Package Pin (Bank | SOM Connector Pin)
-	RGMII TX CLK	O	Transmit Clock: 125MHz in 1000Mbps RGMII mode	**G18** (PS_MIO52 | Bank 502 | SOM 1 D36)
-	RGMII TX CTL	O	Transmit Control	**A16** (PS_MIO57 | Bank 502 | SOM 1 C40)
-	RGMII TX D0	O	Transmit Data 0 from the PS (MAC) to the PHY.	**D16** (PS_MIO53 | Bank 502 | SOM 1 D37)
-	RGMII TX D1	O	Transmit Data 0 from the PS (MAC) to the PHY.	**F17** (PS_MIO54 | Bank 502 | SOM 1 D38)
-	RGMII TX D2	O	Transmit Data 0 from the PS (MAC) to the PHY.	**B16** (PS_MIO55 | Bank 502 | SOM 1 C38)
-	RGMII TX D3	O	Transmit Data 0 from the PS (MAC) to the PHY.	**C16** (PS_MIO56 | Bank 502 | SOM 1 C39)
-	RGMII RX CLK	I	Receive Clock: 125MHz in 1000Mbps RGMII mode	**F18** (PS_MIO58 | Bank 502 | SOM 1 B40)
-	RGMII RX CTL	I	Receive Control	**E18** (PS_MIO63 | Bank 502 | SOM 1 A40)
-	RGMII RX D0	I	Receive Data 0 from the PHY to the PS (MAC).	**E17** (PS_MIO59 | Bank 502 | SOM 1 B41)
-	RGMII RX D1	I	Receive Data 1 from the PHY to the PS (MAC).	**C17** (PS_MIO60 | Bank 502 | SOM 1 B42)
-	RGMII RX D2	I	Receive Data 2 from the PHY to the PS (MAC).	**D17** (PS_MIO61 | Bank 502 | SOM 1 A38)
-	RGMII RX D3	I	Receive Data 3 from the PHY to the PS (MAC).	**A17** (PS_MIO62 | Bank 502 | SOM 1 A39)
-	PHY Reset N	O	Active-low reset to the PHY that initializes or re-initializes all the internal registers	**D19** (PS_MIO69 | Bank 502 | SOM 1 C44)
-	SMI MDC	O	Management Data Clock, synchronous clock to the MDIO (max. 25MHz).	**B20** (PS_MIO76 | Bank 502 | SOM 1 D44)
-	SMI MDIO	I/O	Management Data I/O	**F20** (PS_MIO77 | Bank 502 | SOM 1 D45)

ZM1 (J500) Zmod™ compatible	
Type	QSE-020-01-L-D-A (Samtec: SYZYGY® carrier board standard connector)
Counterpart	QTE-020 (Samtec: SYZYGY® standard connector)
Information	All IO lines are length matched (within <50ps) and impedance controlled 50 Ohm. The slot uses the SYZYGY® standard base board connector and follows the same form factor. The slot is not fully compliant with the SYZYGY standard but remains electrically compatible. SYZYGY® DNA is not supported. All IOs are on 1.8V Banks. The mapping used with two RGMII-PHYs is shown in the datasheets of our ZM Ethernet Modules: ZM ETH 1000 RJ45 ZM ETH 1000 SFP



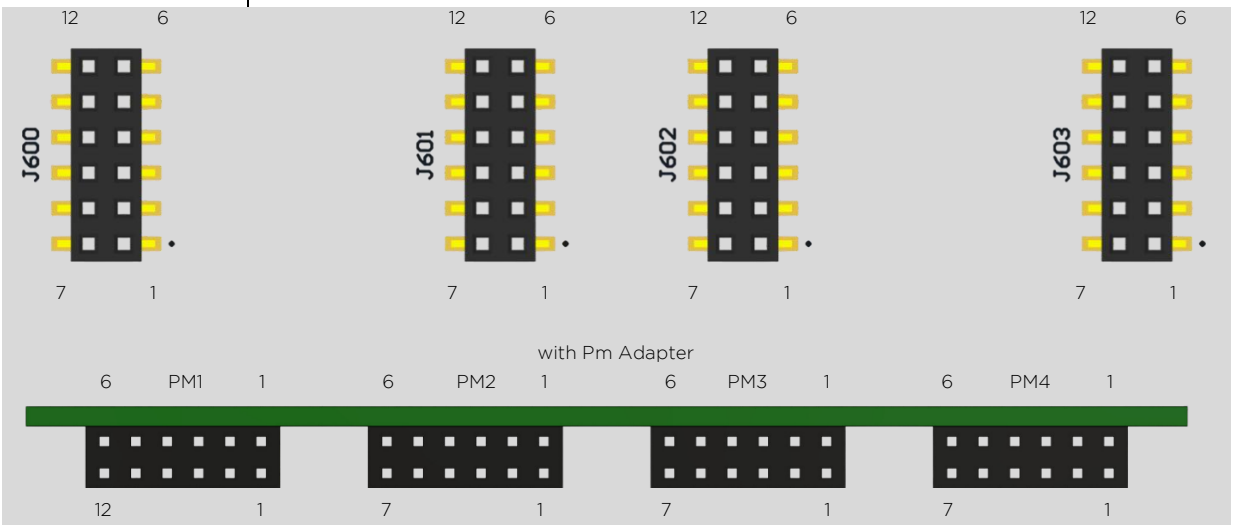
Pin	Signal	I/O	Kria K26 Package Pin (Bank | SOM Connector Pin)	Pin	Signal	I/O	Kria K26 Package Pin (Bank | SOM Connector Pin)
1	NC	-	-	2	5V SOM	I	-
3	NC	-	-	4	R_GA	-	-
5	IO	I/O	**D7** (Bank 66 | SOM 1 C12) Global Clock Pin	6	IO	I/O	**A3** (Bank 66 | SOM 1 B08)
7	IO	I/O	**G8** (Bank 66 | SOM 1 A12)	8	IO	I/O	**B3** (Bank 66 | SOM 1 B07)
9	IO	I/O	**F6** (Bank 66 | SOM 1 A10)	10	IO	I/O	**E3** (Bank 66 | SOM 1 B05)
11	IO	I/O	**G6** (Bank 66 | SOM 1 A09)	12	IO	I/O	**E4** (Bank 66 | SOM 1 B04)
13	IO	I/O	**C2** (Bank 66 | SOM 1 A07)	14	IO	I/O	**B1** (Bank 66 | SOM 1 B02)
15	IO	I/O	**C3** (Bank 66 | SOM 1 A06) Global Clock Pin	16	IO	I/O	**C1** (Bank 66 | SOM 1 B01)
17	IO	I/O	**A1** (Bank 66 | SOM 1 A04)	18	IO	I/O	**D5** (Bank 66 | SOM 1 B11)
19	IO	I/O	**A2** (Bank 66 | SOM 1 A03)	20	IO	I/O	**E5** (Bank 66 | SOM 1 B10) Global Clock Pin
21	IO	I/O	**G1** (Bank 66 | SOM 1 C03)	22	IO	I/O	**D4** (Bank 66 | SOM 1 D10) Global Clock Pin
23	IO	I/O	**F2** (Bank 66 | SOM 1 D04)	24	IO	I/O	**F1** (Bank 66 | SOM 1 C04)
25	IO	I/O	**E2** (Bank 66 | SOM 1 D05)	26	IO	I/O	**G3** (Bank 66 | SOM 1 C06)
27	IO	I/O	**E1** (Bank 66 | SOM 1 D07)	28	IO	I/O	**F3** (Bank 66 | SOM 1 C07)
29	IO	I/O	**D1** (Bank 66 | SOM 1 D08)	30	IO	I/O	**B4** (Bank 66 | SOM 1 C09)
31	IO	I/O	**C4** (Bank 66 | SOM 1 D11)	32	IO	I/O	**A4** (Bank 66 | SOM 1 C10)
33	IO	I/O	**F8** (Bank 66 | SOM 1 D13)	34	IO	I/O	**F7** (Bank 66 | SOM 1 A13)
35	IO	I/O	**E8** (Bank 66 | SOM 1 D14)	36	IO	I/O	**D6** (Bank 66 | SOM 1 C13)
37	Reserved	-	-	38	Reserved	-	-
39	1.8V PL	I	-	40	3.3V PL	I	-

ZM2 (J550) Zmod™ compatible	
Type	QSE-020-01-L-D-A (Samtec: SYZYGY® carrier board standard connector)
Counterpart	QTE-020 (Samtec: SYZYGY® standard connector)
Information	All IO lines are length matched (within <50ps) and impedance controlled 50 Ohm. The slot uses the SYZYGY® standard base board connector and follows the same form factor. The slot is not fully compliant with the SYZYGY standard but remains electrically compatible. SYZYGY® DNA is not supported. All IOs are on 1.8V Banks. The mapping used with two RGMII-PHYs is shown in the datasheets of our ZM Ethernet Modules: ZM ETH 1000 RJ45 ZM ETH 1000 SFP



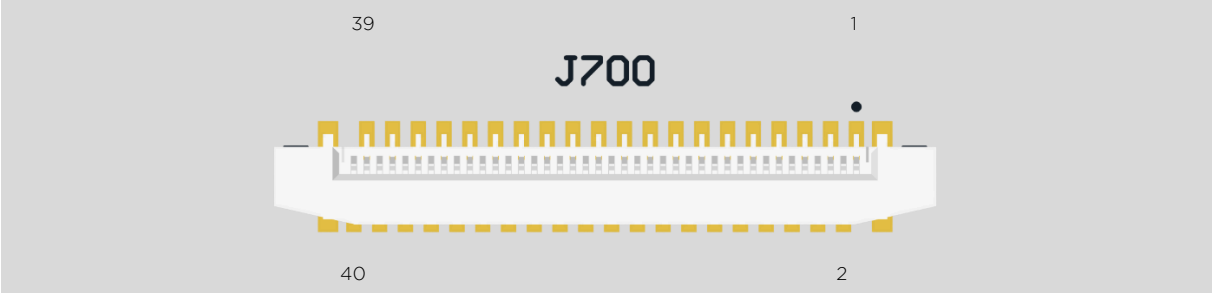
Pin	Signal	I/O	Kria K26 Package Pin (Bank | SOM Connector Pin)	Pin	Signal	I/O	Kria K26 Package Pin (Bank | SOM Connector Pin)
1	NC	-	-	2	5V SOM	I	-
3	NC	-	-	4	R_GA	-	-
5	IO	I/O	**K4** (Bank 65 | SOM 2 C11) Global Clock Pin	6	IO	I/O	**L6** (Bank 65 | SOM 2 B13)
7	IO	I/O	**N7** (Bank 65 | SOM 2 A17)	8	IO	I/O	**N9** (Bank 65 | SOM 2 C14)
9	IO	I/O	**H3** (Bank 65 | SOM 2 A15)	10	IO	I/O	**E3** (Bank 65 | SOM 2 B05)
11	IO	I/O	**H4** (Bank 65 | SOM 2 A14)	12	IO	I/O	**K2** (Bank 65 | SOM 2 B15)
13	IO	I/O	**J5** (Bank 65 | SOM 2 A12)	14	IO	I/O	**J2** (Bank 65 | SOM 2 B16)
15	IO	I/O	**L7** (Bank 65 | SOM 2 B12) Global Clock Pin	16	IO	I/O	**U8** (Bank 65 | SOM 2 C17)
17	IO	I/O	**J5** (Bank 65 | SOM 2 A11)	18	IO	I/O	**V8** (Bank 65 | SOM 2 C18)
19	IO	I/O	**U9** (Bank 65 | SOM 2 D12)	20	IO	I/O	**E5** (Bank 65 | SOM 2 B10) Global Clock Pin
21	IO	I/O	**V9** (Bank 65 | SOM 2 D13)	22	IO	I/O	**M6** (Bank 65 | SOM 2 B21) Global Clock Pin
23	IO	I/O	**W8** (Bank 65 | SOM 2 D15)	24	IO	I/O	**L1** (Bank 65 | SOM 2 B18)
25	IO	I/O	**Y8** (Bank 65 | SOM 2 D16)	26	IO	I/O	**P6** (Bank 65 | SOM 2 C21)
27	IO	I/O	**L2** (Bank 65 | SOM 2 D19)	28	IO	I/O	**L5** (Bank 65 | SOM 2 B22)
29	IO	I/O	**R7** (Bank 65 | SOM 2 D21)	30	IO	I/O	**K9** (Bank 65 | SOM 2 C23)
31	IO	I/O	**T7** (Bank 65 | SOM 2 D22)	32	IO	I/O	**R8** (Bank 65 | SOM 2 B24)
33	IO	I/O	**K8** (Bank 65 | SOM 2 D24)	34	IO	I/O	**J9** (Bank 65 | SOM 2 C24)
35	IO	I/O	**K7** (Bank 65 | SOM 2 D25)	36	IO	I/O	**T8** (Bank 65 | SOM 2 B25)
37	Reserved	-	-	38	Reserved	-	-
39	1.8V PL	I	-	40	3.3V PL	I	-

PM1-PM4 (J600, J601, J602, J603) - Pmod™ compatible	
Type	SSM-106-L-DV (Samtec: Straight Pmod Connector)
Counterpart	Standard 6/12-pin male connector 2.54mm pitch according to Digilent Pmod™ Interface Specification.
Information	The Pm slots are designed and the IOs numbered to use in combination with the AIONYX PM Adapter. Check the IO numbering carefully. The slots are Pmod™ compatible according to the Digilent Pmod™ Interface Specification. All IOs are on 3.3V Banks.



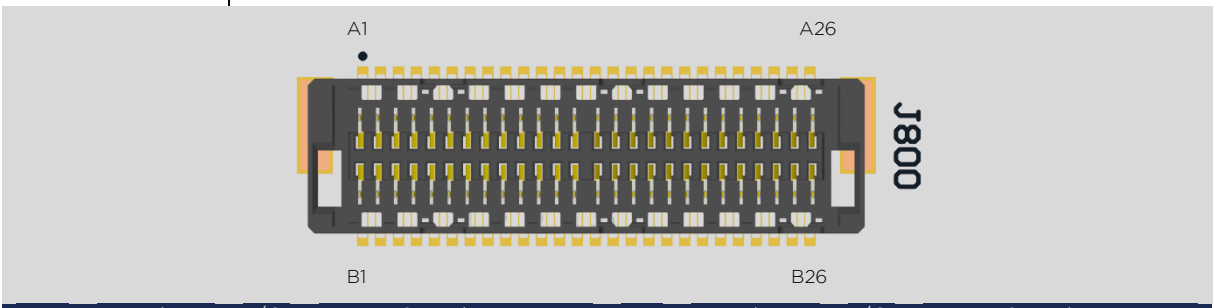
Pin	Signal	I/O	Kria K26 Package Pin (Bank | SOM Connector Pin)	Pin	Signal	I/O	Kria K26 Package Pin (Bank | SOM Connector Pin)
PM1 (J600)							
1	IO1	I/O	**G11** (Bank 45 | SOM 1 D16) Global Clock Pin	7	IO5	I/O	**F10** (Bank 45 | SOM 1 D17)
2	IO2	I/O	**J11** (Bank 45 | SOM 1 D18)	8	IO6	I/O	**H11** (Bank 45 | SOM 1 C18)
3	IO3	I/O	**C11** (Bank 45 | SOM 1 D22)	9	IO7	I/O	**G10** (Bank 45 | SOM 1 C19)
4	IO4	I/O	**D10** (Bank 45 | SOM 1 D21)	10	IO8	I/O	**E10** (Bank 45 | SOM 1 D20)
5	GND	-	-	11	GND	-	-
6	VCC (3.3V PL)	O	-	12	VCC (3.3V PL)	O	-
PM2 (J601)							
1	IO1	I/O	**E12** (Bank 45 | SOM 1 B21) Global Clock Pin	7	IO5	I/O	**E12** (Bank 45 | SOM 1 B21)
2	IO2	I/O	**B11** (Bank 45 | SOM 1 C22)	8	IO6	I/O	**B11** (Bank 45 | SOM 1 C22)
3	IO3	I/O	**A10** (Bank 45 | SOM 1 C23)	9	IO7	I/O	**A10** (Bank 45 | SOM 1 C23)
4	IO4	I/O	**A12** (Bank 45 | SOM 1 C24)	10	IO8	I/O	**A12** (Bank 45 | SOM 1 C24)
5	GND	-	-	11	GND	-	-
6	VCC (3.3V PL)	O	-	12	VCC (3.3V PL)	O	-
PM3 (J602)							
1	IO1	I/O	**AD11** (Bank 43 | SOM 2 B44) Global Clock Pin	7	IO5	I/O	**AE12** (Bank 43 | SOM 2 D44)
2	IO2	I/O	**AA11** (Bank 43 | SOM 2 B46)	8	IO6	I/O	**AH12** (Bank 43 | SOM 2 C46)
3	IO3	I/O	**AA10** (Bank 43 | SOM B48)	9	IO7	I/O	**AC11** (Bank 43 | SOM 2 B50)
4	IO4	I/O	**AH11** (Bank 43 | SOM 2 C47)	10	IO8	I/O	**AF10** (Bank 43 | SOM 2 C52)
5	GND	-	-	11	GND	-	-
6	VCC (3.3V PL)	O	-	12	VCC (3.3V PL)	O	-
PM4 (J603)							
1	IO1	I/O	**AB11** (Bank 43 | SOM 2 B49) Global Clock Pin	7	IO5	I/O	**AB9** (Bank 43 | SOM 2 A52)
2	IO2	I/O	**AB10** (Bank 43 | SOM 2 D51)	8	IO6	I/O	**Y10** (Bank 43 | SOM 2 A47)
3	IO3	I/O	**AA8** (Bank 43 | SOM 2 A50)	9	IO7	I/O	**W10** (Bank 43 | SOM 2 46)
4	IO4	I/O	**Y9** (Bank 43 | SOM 2 A48)	10	IO8	I/O	**AD10** (Bank 43 | SOM 2 B45)
5	GND	-	-	11	GND	-	-
6	VCC (3.3V PL)	O	-	12	VCC (3.3V PL)	O	-

Flex Connector (J700)	
Type	52559-4052 (Molex: FFC/FPC Connector)
Counterpart	40 pin FlexPrint 0.5mm pitch
Information	All IOs are on 1.8V Banks.



Pin	Signal	I/O	Kria K26 Package Pin (Bank | SOM Connector Pin)	Pin	Signal	I/O	Kria K26 Package Pin (Bank | SOM Connector Pin)
1	1.8V PL	O	-	2	1.8V PL	O	-
3	1.8V PL	O	-	4	GND	-	-
5	3.3V PL	O	-	6	3.3V PL	O	-
7	3.3V PL	O	-	8	GND	-	-
9	5V SOM	O	-	10	5V SOM	O	-
11	5V SOM	O	-	12	GND	-	-
13	IO	I/O	**AC2** (Bank 64 | SOM 2 A36)	14	IO	I/O	**AE7** (Bank 64 | SOM 2 A42)
15	IO	I/O	**AB2** (Bank 64 | SOM 2 A35)	16	IO	I/O	**AD7** (Bank 64 | SOM 2 A41)
17	IO	I/O	**AG6** (Bank 64 | SOM A29)	18	IO	I/O	**AF2** (Bank 64 | SOM 2 B40)
19	IO	I/O	**H8** (Bank 65 | SOM 2 A27)	20	IO	I/O	**AH4** (Bank 64 | SOM 2 A39)
21	IO	I/O	**AE2** (Bank 64 | SOM 2 B39)	22	IO	I/O	**AG4** (Bank 64 | SOM 2 A38)
23	IO	I/O	**AH7** (Bank 64 | SOM 2 B37)	24	IO	I/O	**H9** (Bank 65 | SOM 2 A26)
25	IO	I/O	**AH8** (Bank 64 | SOM 2 B36)	26	IO	I/O	**H7** (Bank 65 | SOM 2 A24)
27	IO	I/O	**AH3** (Bank 64 | SOM 2 B34)	28	IO	I/O	**J7** (Bank 65 | SOM 2 A23)
29	IO	I/O	**AG3** (Bank 64 | SOM 2 B33)	30	IO	I/O	**AH1** (Bank 64 | SOM A33)
31	IO	I/O	**AD1** (Bank 64 | SOM 2 B31)	32	IO	I/O	**AH2** (Bank 64 | SOM 2 A32)
33	IO	I/O	**AG8** (Bank 64 | SOM 2 B28)	34	IO	I/O	**AG5** (Bank 64 | SOM 2 A30)
35	IO	I/O	**AF8** (Bank 64 | SOM 2 B27)	36	IO	I/O	**H1** (Bank 65 | SOM 2 A21)
37	IO	I/O	**AF3** (Bank 64 | SOM 2 C27)	38	IO	I/O	**J1** (Bank 65 | SOM 2 A20)
39	IO	I/O	**AE3** (Bank 64 | SOM 2 C26)	40	IO	I/O	**N6** (Bank 65 | SOM 2 A18)

Backplane Connector (J800)	
Type	1154077 (PHOENIX CONTACT)
Counterpart	1061729 (PHOENIX CONTACT)
Information	Pin B11 to B18 are differential Ethernet Lines, connected to Magnetics on the Carrier Board. How the PHY (U800 DP83869HM) is connected to the FPGA can be found directly below. The PHY has the SMI Address 0x0C. All IOs are on 3.3V Banks, the connection to the PHY is on a 1.8V Bank.



Pin	Signal	I/O	Kria K26 Package (Bank | SOM Connector Pin)	Pin	Signal	I/O	Kria K26 Package (Bank | SOM Connector Pin)
A1	GND	-		B1	GND	-	-
A2	IO	I/O	**AC13** (Bank 44 | SOM 2 C58)	B2	IO	I/O	**AH14** (Bank 44 | SOM 2 D58)
A3	IO	I/O	**AE13** (Bank 44 | SOM 2 C59)	B3	IO	I/O	**AG14** (Bank 44 | SOM 2 D57)
A4	IO	I/O	**AF13** (Bank 44 | SOM 2 C60)	B4	IO	I/O	**AE14** (Bank 44 | SOM 2 D56)
A5	IO	I/O	**W11** (Bank 44 | SOM 2 A58)	B5	IO	I/O	**AC14** (Bank 44 | SOM 2 C56) Global Clock Pin
A6	IO	I/O	**AB14** (Bank 44 | SOM 2 B58)	B6	IO	I/O	**AH13** (Bank 44 | SOM 2 C55)
A7	IO	I/O	**AB15** (Bank 44 | SOM 2 B57) Global Clock Pin	B7	IO	I/O	**AE15** (Bank 44 | SOM 2 D54)
A8	IO	I/O	**W12** (Bank 44 | SOM 2 A56)	B8	IO	I/O	**AG13** (Bank 44 | SOM 2 C54)
A9	IO	I/O	**Y13** (Bank 44 | SOM 2 A55)	B9	IO	I/O	**AD14** (Bank 44 | SOM 2 D53)
A10	IO	I/O	**Y14** (Bank 44 | SOM 2 A54)	B10	IO	I/O	**AD15** (Bank 44 | SOM 2 D52) Global Clock Pin
A11	IO	I/O	**AE10** (Bank 43 | SOM 2 C51)	B11	ETH TD A P	I/O	**-**
A12	IO	I/O	**AD12** (Bank 43 | SOM 2 C50)	B12	ETH TD A N	I/O	**-**
A13	IO	I/O	**AG11** (Bank 43 | SOM 2 D50)	B13	ETH TD B P	I/O	**-**
A14	IO	I/O	**AF11** (Bank 43 | SOM 2 D49)	B14	ETH TD B P	I/O	**-**
A15	IO	I/O	**AC12** (Bank 43 | SOM 2 C48) Global Clock Pin	B15	ETH TD C P	I/O	**-**
A16	IO	I/O	**AH10** (Bank 43 | SOM 2 D48)	B16	ETH TD C N	I/O	**-**
A17	IO	I/O	**AG10** (Bank 43 | SOM 2 D46)	B17	ETH TD D P	I/O	**-**
A18	IO	I/O	**AF12** (Bank 43 | SOM 2 D45) Global Clock Pin	B18	ETH TD D N	I/O	**-**
A20	1.8V	I/O	-	B20	1.8V	I/O	-
A21	1.8V	I/O	-	B21	1.8V	I/O	-
A22	5V	I/O	-	B22	5V	I/O	-
A23	5V	I/O	-	B23	5V	I/O	-
A24	3.3V	I/O	-	B24	3.3V	I/O	-
A25	3.3V	I/O	-	B25	3.3V	I/O	-
A25	ResetN	I/O	-	B25	Power Good	I/O	-
A26	GND	-	-	B26	GND	-	-

Backplane Ethernet PHY (U800 DP83869HM)

Pin	Signal	I/O	Description	Kria K26 Package Pin (Bank | SOM Connector Pin)
-	RGMII TX CLK	O	Transmit Clock: 125MHz in 1000Mbps RGMII mode	**AC9** (Bank 64 | SOM 2 D33)
-	RGMII TX CTL	O	Transmit Control	**AC8** (Bank 64 | SOM 2 D37)
-	RGMII TX D0	O	Transmit Data 0 from the FPGA (MAC) to the PHY.	**AC4** (Bank 64 | SOM 2 C32)
-	RGMII TX D1	O	Transmit Data 0 from the FPGA (MAC) to the PHY.	**AE8** (Bank 64 | SOM 2 D31)

-	RGMII TX D2	O	Transmit Data 0 from the FPGA (MAC) to the PHY.	**AE9** (Bank 64 | SOM 2 D30)
-	RGMII TX D3	O	Transmit Data 0 from the FPGA (MAC) to the PHY.	**AF6** (Bank 64 | SOM 2 D28)
-	RGMII RX CLK	I	Receive Clock: 125MHz in 1000Mbps RGMII mode	**AD5** (Bank 64 | SOM 2 C29)
-	RGMII RX CTL	I	Receive Control	**AC8** (Bank 64 | SOM 2 D37)
-	RGMII RX D0	I	Receive Data 0 from the PHY to the FPGA (MAC).	**AD9** (Bank 64 | SOM 2 D34)
-	RGMII RX D1	I	Receive Data 1 from the PHY to the FPGA (MAC).	**AB4** (Bank 64 | SOM 2 C35)
-	RGMII RX D2	I	Receive Data 2 from the PHY to the FPGA (MAC).	**AB3** (Bank 64 | SOM 2 C36)
-	RGMII RX D3	I	Receive Data 3 from the PHY to the FPGA (MAC).	**AB8** (Bank 64 | SOM 2 D36)
-	PHY Reset N	O	Active-low reset to the PHY that initializes or re-initializes all the internal registers	**AC7** (Bank 64 | SOM 2 D40)
-	PHY CLK IN	O	25 MHz Clock Input on the PHY (Provided by FPGA)	**AG9** (Bank 64 | SOM 2 C37)
	PHY CLK Out	I	25 MHz Clock Output from PHY (Clock Pin on FPGA)	**AF7** (Bank 64 | SOM 2 D27)
-	SMI MDC	O	Management Data Clock, synchro-nous clock to the MDIO (max. 25MHz).	**AE5** (Bank 64 | SOM 2 C41)
-	SMI MDIO	I/O	Management Data I/O	**AH9** (Bank 64 | SOM 2 C39)

Board-Internal Devises, Interfaces and Pin Description

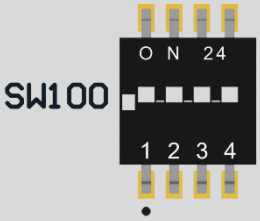
Oscillator (Y100)

Type	TG3225CEN 25.0000 MHz +/-2.0PPM (EPSON)

Pin	Signal	I/O	Description	Kria K26 Package Pin (Bank | SOM Connector Pin)
3	Out	I	25MHz Clock Out of the Oscillator	**F12** (Bank 45 | SOM 1 C20)

Boot Mode Configuration (SW100)

Type	DIP Switch 4 Positions
Configuration	Supported Configuration for Boot Mode Pins [3:0]: `0000`: PS JTAG `0001`: Quad-SPI (24b) (MIO[12 :0]) `0010`: Quad-SPI (32b) (MIO[12 :0]) `0101`: SD1 (2.0) (MIO[51:43]) **DEFAULT** `0110`: eMMC (1.8V) (MIO[22:13]) ON-Symbol on the DIP Switch means closed and the Mode is pulled to Ground → 0.



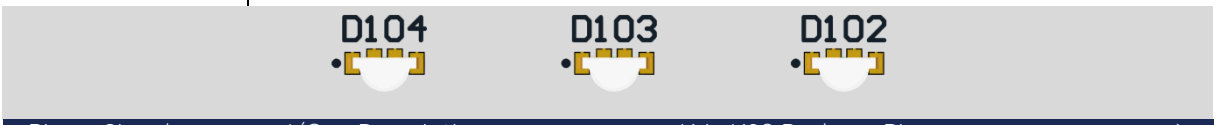
Pin	Signal	I/O	Description	Kria K26 Package Pin (Bank | SOM Connector Pin)
1	MODE0_C2M	I	PS mode bit 0	**P19** (Bank 503 | SOM 1 A27)
2	MODE1_C2M	I	PS mode bit 1	**P20** (Bank 503 | SOM 1 A28)
3	MODE2_C2M	I	PS mode bit 2	**R20** (Bank 503 | SOM 1 A29)
4	MODE3_C2M	I	PS mode bit 3	**T20** (Bank 503 | SOM 1 A30)

User LEDs (D100 & D101)

Type	Green LED

Pin	Signal	I/O	Description	Kria K26 Package Pin (Bank | SOM Connector Pin)
-	LED0	O	User LED 0	**Y12** (Bank 44 | SOM 1 A59)
-	LED1	O	User LED 1	**AA12** (Bank 44 | SOM 1 A60)

User RGB LEDs (D102, D103, D104)	
Type	155124M173200 Side View RGB LED (Würth)
Information	Pulling to 0 turns the LED on The Green LED of D102 is directly connected to the FPGA. All other LEDs can be controlled via the I2C IO Expander TCA9554DBR (U100). The IO Expander has the I2C Address 0x20. Expander Ports P0: LED D103 Green P1: LED D103 Red P2: LED D102 Blue P3: LED D102 Red P4: LED D103 Blue P5: LED D104 Red P6: LED D104 Green P7: LED D104 Blue



Pin	Signal	I/O	Description	Kria K26 Package Pin (Bank | SOM Connector Pin)
-	LED I2C SCL	O	I2C serial clock bus	**AB13** (Bank 44 | SOM 1 A27)
-	LED I2C SDA	I/O	I2C serial data bus	**W14** (Bank 44 | SOM 1 A28)
-	LED D102 Green	O	Direct connected to the green LED	**AA13** (Bank 44 | SOM 1 A28)

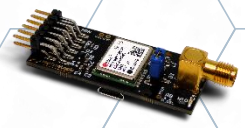
PS I2C Devices (U300, U301)	
Type	24CW1280T-I/OT (Microchip EEPROM), TMP1075DR (Ti Temperature Sensor)
Information	On the I2C Bus interface of the PS are two devices connected. An EEPROM (I2C Addr: 0x50) and a Temperature Sensor (I2C Addr: 0x48)

Pin	Signal	I/O	Description	Kria K26 Package Pin (Bank | SOM Connector Pin)
-	PS I2C SCL	O	I2C serial clock bus	**AB19** (PS_MIO24 | Bank 500 | SOM 1 C26)
-	PS I2C SDA	I/O	I2C serial data bus	**AB21** (PS_MIO25 | Bank 500 | SOM 1 C27)

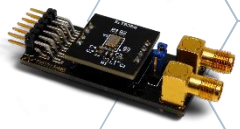
PM Module Options

PM Furuno GT88

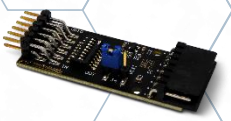
PM ComNav K801



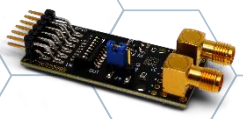
PM u-blox M9N



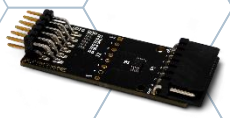
PM CLK RTC



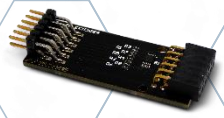
PM GPIO



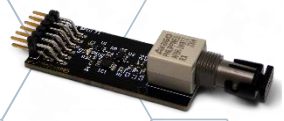
PM GPIO SMA



PM GPIO RAW

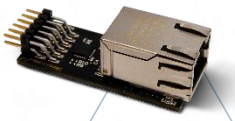


PM Extender

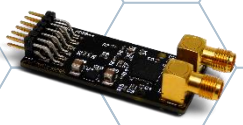


PM GPIO FI

PM GPIO FO

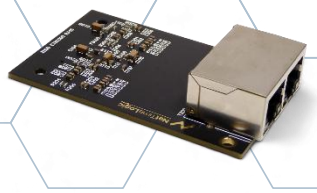


PM ETH



PM AD9544

ZM Module Options



ZM ETH 1000 RJ45

ZM ETH 1000 SFP

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