

IrigSlaveClock

A low-footprint, highly configurable, 100% hardware only IRIG Slave Clock solution, specifically designed for high-performance distributed systems. Allows standalone synchronization with compensation of cable and input circuit delays and time base correction to work with UTC or TAI time bases.

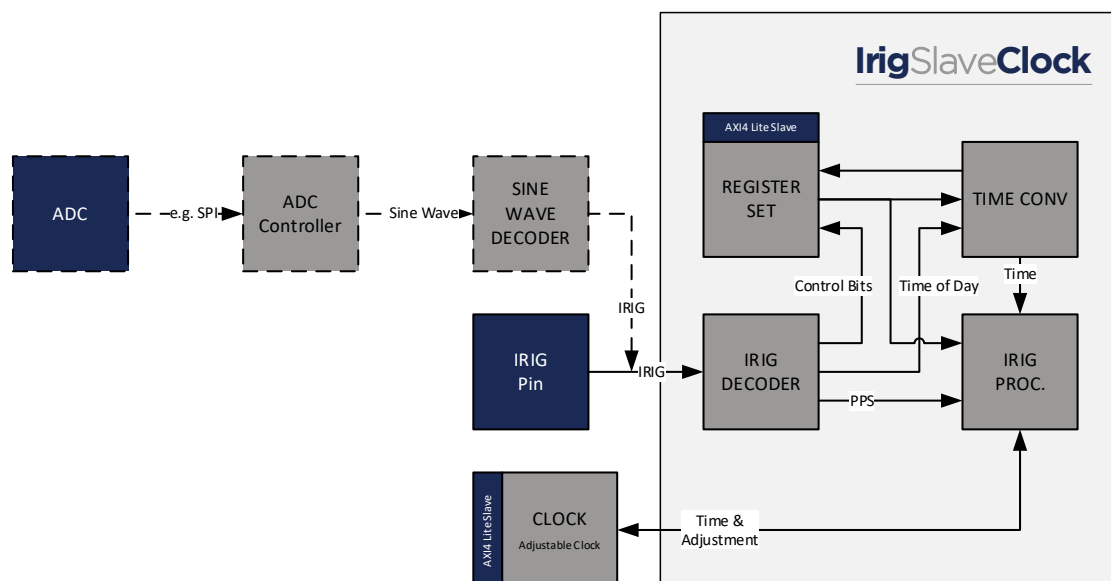
Key Features:

- IRIG-B006/G006 Slave Clock (IRIG-B126/G146 with ADC)
- Extraction of Control Bits
- 100% hardware only solution
- Vendor independent
- Time base correction
- Cable and Input delay compensation
- PI Servo Loop in hardware
- Time frame encoding

Typical Applications:

- Legacy Networks
- Time converters
- Robot control
- Substation automation
- Distributed data acquisition
- Test and measurement
- Etc.

IP Core Architecture:



Specification:

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|---------------|--|
| IRIG | <p>IRIG synchronization, supports IRIG-B006/G006 format (compatible with B004, B005, B006 and B007 IRIG-B Masters)</p> <p>PWM and DCLS decoding for IRIG-B006 and IRIG-G006</p> <p>AC and AM decoding with ADC for IRIG-B126 and IRIG-G146 (IRIG-G requires ≥ 1MSPL ADC)</p> <p>Extracts Control Bits and provides it to user</p> <p>Time base conversion from TAI to UTC (or any other time base)</p> <p>Time frame encoding and supervision in hardware</p> <p>Compensation of input circuits and cable delays</p> <p>Cable delays can be changed at runtime</p> <p>Offset and drift calculation for adjusting the clock</p> |
| Performance | <p>Timestamp accuracy of rising edge IRIG +/- an input clock period, offload synchronization</p> |
| Portability | <p>100% hardware only solution, no dependency on external CPU or external driver circuitry features</p> <p>Vendor independent, written in plain VHDL</p> <p>Low footprint and low frequency requirements</p> |
| Modularity | <p>Slim and standardized interfaces are used</p> |
| Configuration | <p>No CPU required, standalone configuration with signals</p> <p>Axi4 lite slave support, for status and configuration</p> |

Deliverables:

- Ip core in plain VHDL
- Testbench in plain VHDL
- Reference Design with 1 IRIG input and 1 PPS output
 - Top level VHDL file
 - Timing Constraint SDC files
 - Vivado/Quartus Project file

Related Products:

- PTP Ordinary Clock
- PTP Grandmaster Clock
- PTP Hybrid Clock
- IRIG Master
- IRIG Master/Slave
- Adjustable Clock
- Signal Timestamper
- Signal Generator



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