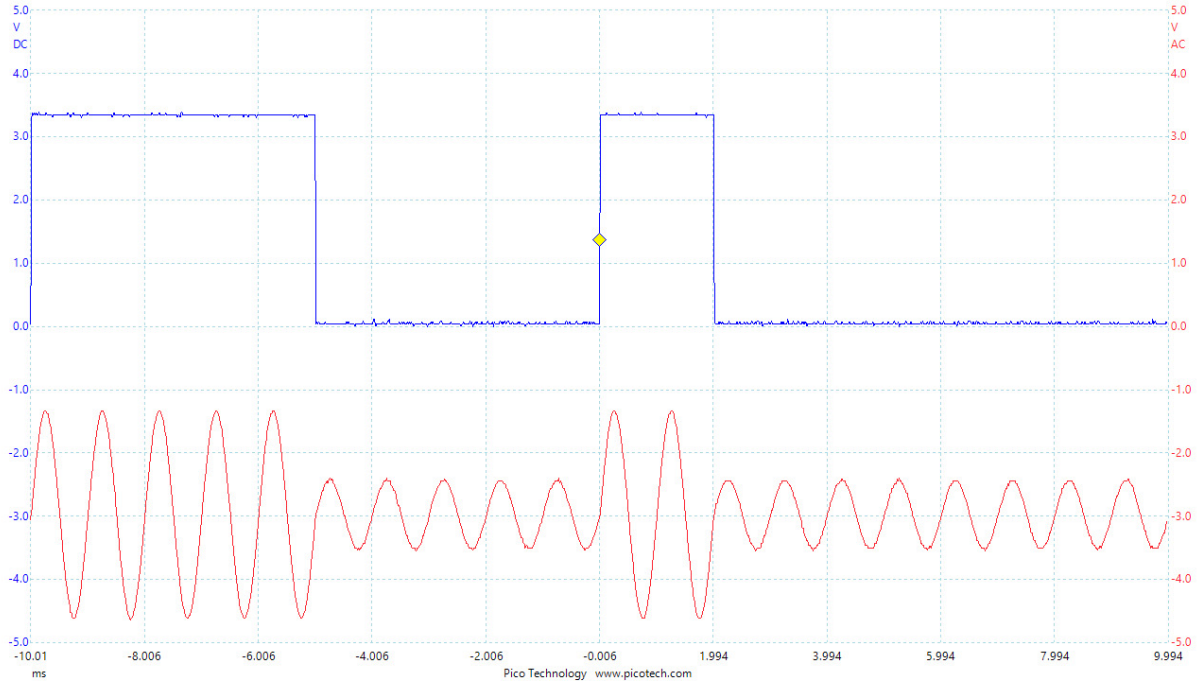


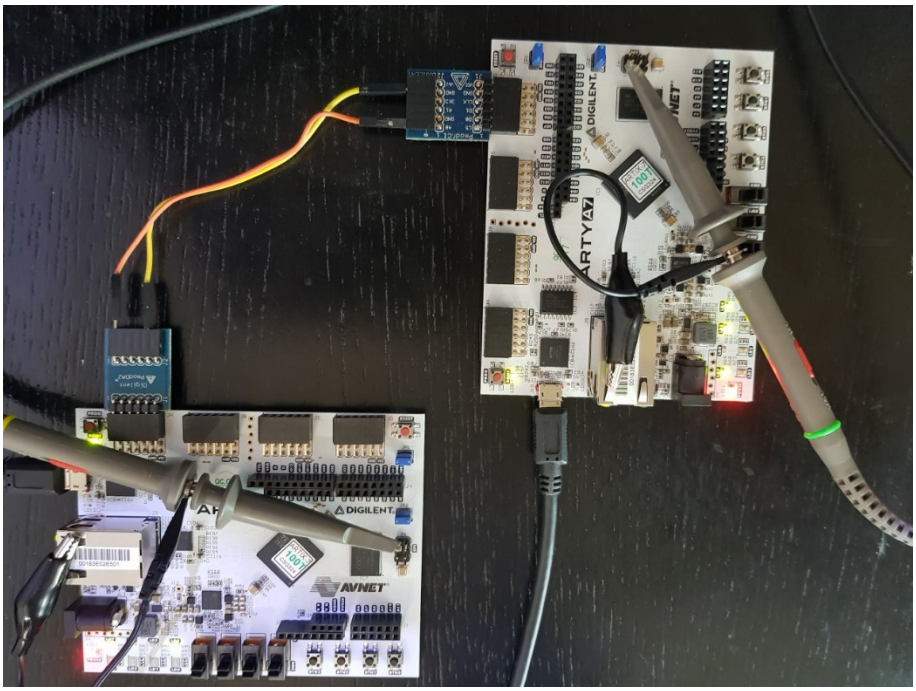
IRIG-B12x with DAC and ADC

27. August 2018

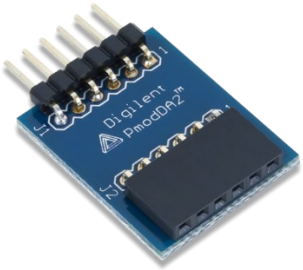
NetTimeLogic just released the AC amplitude modulated versions of its IRIG Master and IRIG Slave IP cores and we will give you some insight to our solution. In this post we want to explain how high accuracy (<2 us) IRIG-B12x (sine wave encoded, amplitude modulated IRIG-B) can be implemented using cheap DACs and ADCs. As with all NetTimeLogic IP cores this is also an FPGA only solution (no software required), however some additional Analog/Digital converter chips are required. The goal of this solution is to get highest accuracy synchronization, with minimal costs.

The solution is using external DACs (Digital to Analog Converter, Digilent PmodDA2) and ADCs (Analog to Digital Converter, Digilent PmodAD1) for the handling of the analog sine wave of IRIG-B12X.

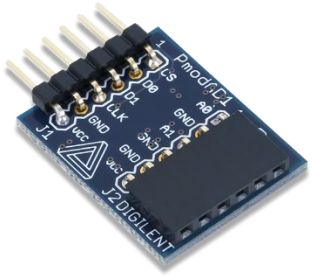
This is how our setup looks like: We use two Digilent ArtyA7-100 for our development, one is acting as an IRIG Master (with the DAC), the other is acting as an IRIG Slave (with the ADC) and we are comparing the PPS (Pulse Per Second) from the two counter clocks which are synchronized via IRIG-B127



The PmodDA2 module is a Digital to Analog Converter board from Digilent in a PMOD format featuring a Texas Instruments DAC121S101 DAC which is a 12bit DAC with a maximum sample rate of 1 mega sample per second and a SPI like interface.

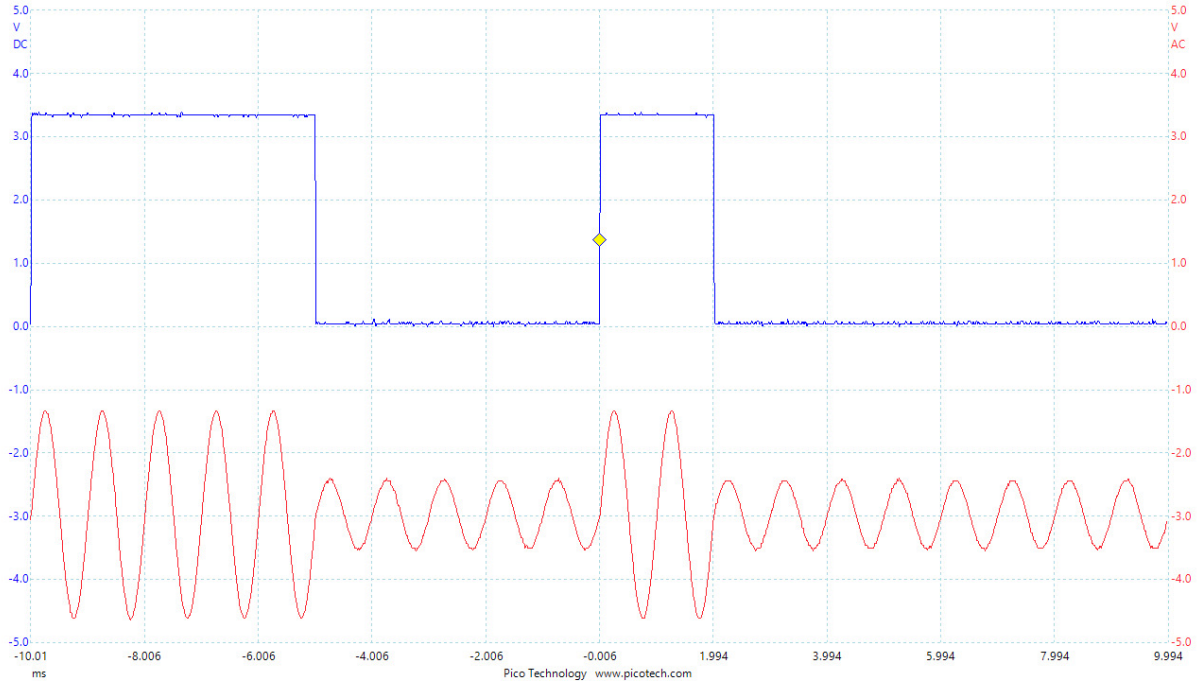


The PmodAD1 module is a Analog to Digital Converter board from Digilent in a PMOD format featuring a Analog Devices AD7476A ADC which is a 12bit ADC with a maximum sample rate of 1 mega sample per second and a SPI like interface.



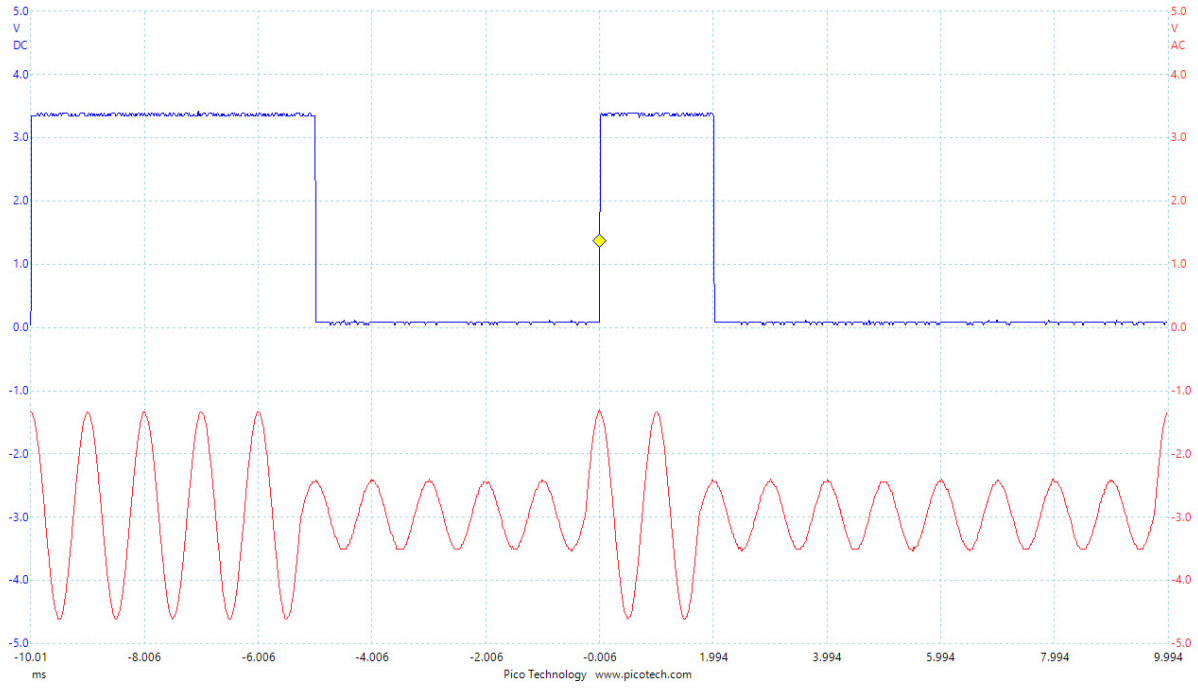
The sine wave encoding and decoding as well as the ADC and DAC controllers are completely independent modules in the FPGA.

On the DAC side, the encoder takes a DCLS (DC level shift) IRIG-B signal coming from the NetTimeLogic IRIG Master and converts it into an aligned (with the local counter clock) sine wave signal as samples of N bits (configurable depending on the DAC) with a modulated amplitude for 0/1 encoding for the DAC. The number of samples per sine wave period and bits per sample are configurable to allow all kind of DACs. The amplitude is encoded in a way that it uses the full DAC range for a logic one and 1/3 of the amplitude for a logic zero. Then a simple SPI controller is triggered for each sample which it then feeds to the DAC over a SPI like interface at 12.5MHz. With this setup a sample rate of 500kHz (based on the counter clock) is used.
The picture below shows how the IRIG-B00x signal is aligned with the generated IRIG-B12x signal. Amplitude changes happen at the level change of the DC signal. The analog signal is slightly shifted by the DAC delay for the conversion and the SPI access. This delay can be configured in the NetTimeLogic IRIG Master as output delay and will be compensated accordingly, so the sine wave is perfectly aligned with the counter clock.

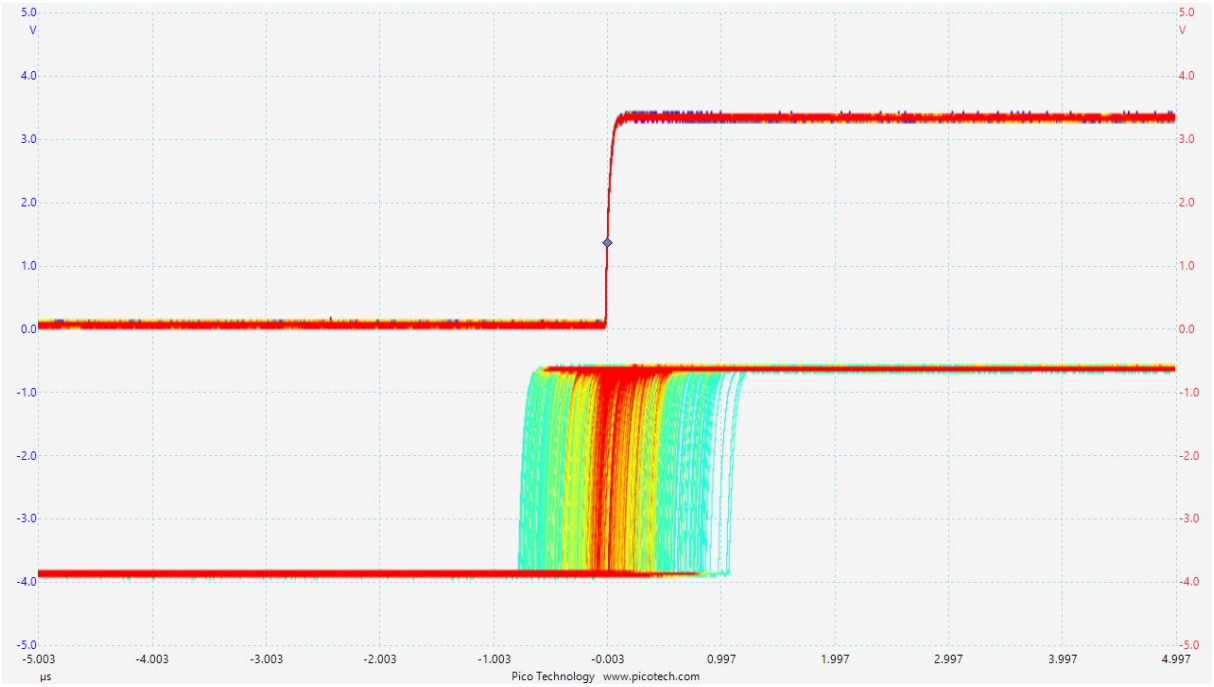


On the ADC side, a simple SPI controller reads the voltage value from the ADC via an SPI like interface every 2 us (based on the local clock) which equals to a sample rate of 500kHz. These samples are then feed to the decoder. The decoder does an

automatic signal, offset, range and zero crossing detection and converts the sine wave samples into a DCLS IRIG-B signal which is then feed as input to the NetTimeLogic IRIG Slave.
The picture below shows how the IRIG-B12x signal is aligned with the decoded IRIG-B00x signal. DCLS changes happen 1/4 of a sine wave period after the zero crossing of the sine wave (at the first positive peak after the zero crossing). This because this is the first deterministic point where the amplitude can be checked to determine if a zero or one was modulated. This constant offset is no issue, since in the NetTimeLogic IRIG Slave this value can be configured as input delay and will be compensated for accordingly. Additionally the ADC delay for the conversion and reading over SPI shall be added to the input delay to achieve high accuracy synchronization without offset.



The synchronization accuracy can be checked by comparing the PPS of the two modules which are fed to a pin. A rising edge marks the beginning of a new second on the counter clock.
With the setup described above a synchronization accuracy of less than 1.5us can be achieved.



For more information check www.nettimlogic.com

After some fine tuning of the servo parameters the accuracy has improved to less than +/- 800ns. Since the detection of the zero crossing highly depends on the accuracy of the ADC, noise and the sampling rate, different PI servo parameters were chosen to make it slower and filter out this sources of inaccuracy.