

DcfSlaveClock

A low-footprint, highly configurable, 100% hardware only DCF Slave Clock solution, specifically designed for high-performance distributed systems. Allows standalone synchronization with compensation of air propagation and input circuit delays and time base correction to work with UTC or TAI time bases.

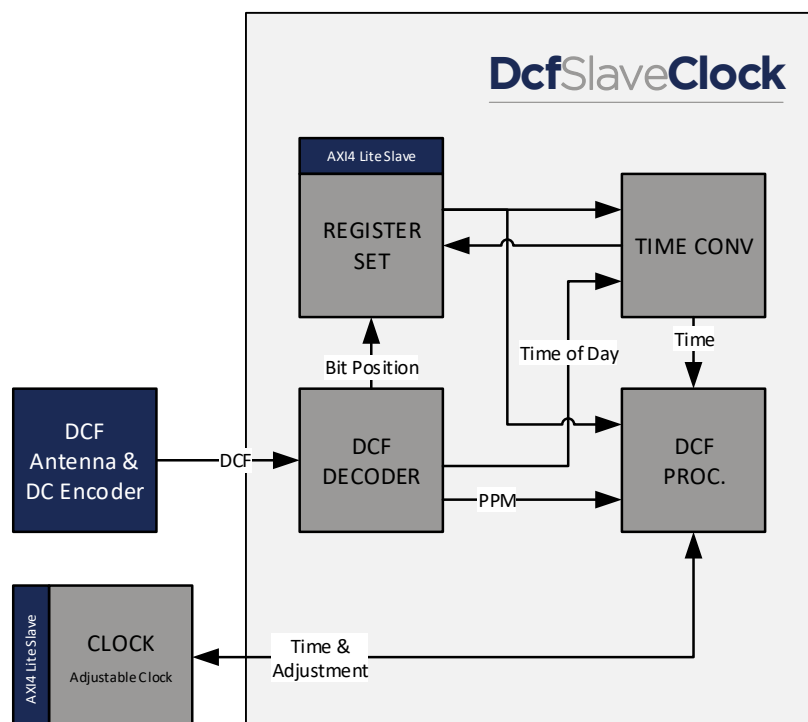
Key Features:

- DCF-77 Slave Clock
- 100% hardware only solution
- Vendor independent
- Time base correction
- Air propagation and Input delay compensation
- PI Servo Loop in hardware
- Optional Signal Filter
- Time frame encoding

Typical Applications:

- Legacy Networks
- Time converters
- Robot control
- Substation automation
- Distributed data acquisition
- Test and measurement
- Etc.

IP Core Architecture:



Specification:

DCF	DCF synchronization, PWM encoding. Supports DCF-77 Time base conversion from TAI to UTC (or any other time base) Time frame encoding and supervision in hardware Compensation of input circuits and air propagation delays Air propagation delay can be changed at runtime Offset and drift calculation for adjusting the clock
Performance	Timestamp accuracy of rising edge DCF +/- an input clock period, +/-10 ms accuracy, offload synchronization
Portability	100% hardware only solution, no dependency on external CPU Vendor independent, written in plain VHDL Low footprint and low frequency requirements
Modularity	Slim and standardized interfaces are used
Configuration	No CPU required, standalone configuration with signals Axi4 lite slave support, for status and configuration

Deliverables:

- Ip core in plain VHDL
- Testbench in plain VHDL
- Reference Design with 1 DCF input and 1 PPS output
 - Top level VHDL file
 - Timing Constraint SDC files
 - Vivado/Quartus Project file

Related Products:

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|-------------------------|----------------------|
| • PTP Ordinary Clock | • IRIG Master/Slave |
| • PTP Grandmaster Clock | • Adjustable Clock |
| • PTP Hybrid Clock | • Signal Timestamper |
| • PPS Master | • Signal Generator |



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