Dcf MasterClock

A low-footprint, highly configurable, 100% hardware only DCF Master Clock solution, specifically designed for high-performance distributed systems. Allows compensating driver circuit delays and time base correction to distribute UTC or TAI time.
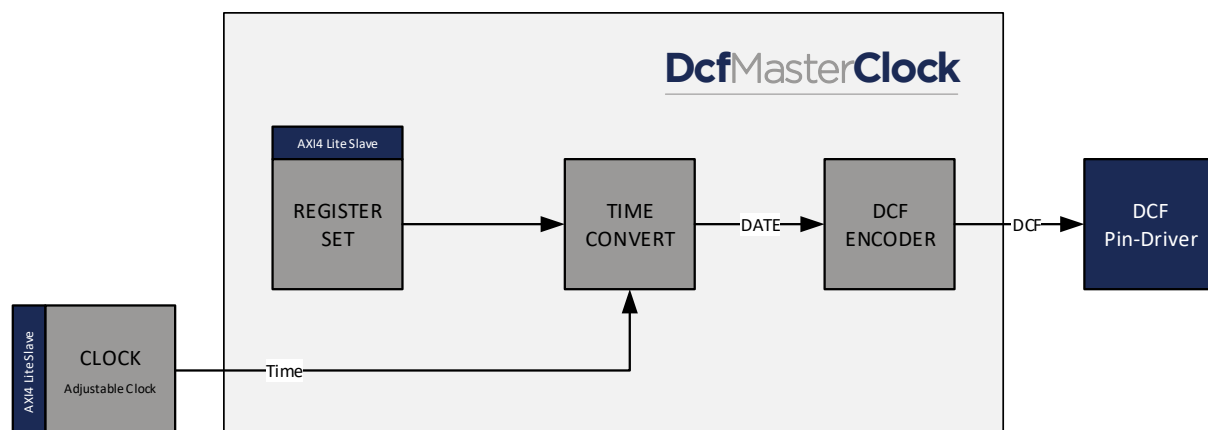
Key Features:

- DCF-77 Master Clock
- 100% hardware only solution
- Vendor independent
- Output delay compensation
- Time base correction
- High precision DCF generation aligned with local clock

Typical Applications:

- Legacy Networks
- Time converters
- Robot control
- Substation automation
- Distributed data acquisition
- Test and measurement
- Etc.

IP Core Architecture:

Specification:

DCF	DCF synchronization, PWM encoding. Supports DCF-77 including weekdays
	Time base conversion from TAI to UTC (or any other time base)
	Reference Mark Symbol aligned with NetTimeLogic's Clock
	Output delay compensation
Performance	Accuracy of rising edge DCF +/- an input clock period,
	Symbol times also aligned with the clock
Portability	100% hardware only solution, no dependency on external CPU or external driver circuitry features
	Vendor independent, written in plain VHDL
	Low footprint and low frequency requirements
Modularity and scalability	Simple time format can be also sourced by third-party clock core
	Slim and standardized interfaces are used
Configuration	No CPU required, standalone configuration with signals
	Axi4 lite slave support, for status and configuration

Deliverables:

- Ip core in plain VHDL
- Testbench in plain VHDL
- Reference Design with 1 DCF output and 1 PPS output
    - o Top level VHDL file
    - o Timing Constraint SDC files
    - o Vivado/Quartus Project file

Related Products:

- PTP Ordinary Clock
- PTP Grandmaster Clock
- PTP Hybrid Clock
- DCF Slave

- IRIG Master/Slave
- Adjustable Clock
- Signal Timestamper
- Signal Generator

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