ClockSignalTimestamper

A low-footprint signal timestamper which uses NetTimeLogic's clock IP core as source for timestamping. Together with the signal to timestamp, data can be provided which will then be latched, so that the timestamp and data can be aligned with each other. For burst handling, an optional timestamp buffer can be enabled. Timestamps will generate an IRQ and can be read via AXI4.

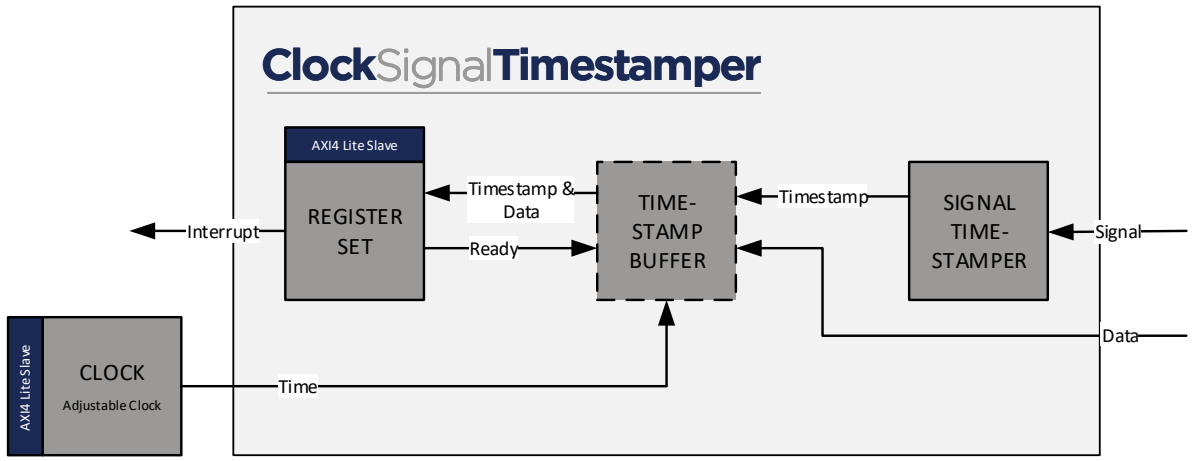
Key Features:

- Asynchronous timestamping
- Data alignment with timestamping
- Timestamp buffering for burst handling
- IRQ generation
- AXI4 lite slave interface
- Max signal toggle frequency limited by register access speed
- Optional TDC for 1ns accuracy

Typical Applications:

- Distributed data acquisition
- Test and measurement
- Robot control
- Substation automation
- Ethernet based automation networks
- Etc.

IP Core Architecture:



Specification:

Timestamping	Timestamp resolution is one clock cycle of the adjustable clock IP core without oversampling clock or one clock cycle of the over-sampling clock or 1 ns with TDC. Meta stability flip flops for asynchronous signal handling Input delay compensation takes also external delays into ac-count. Timestamping generates interrupts Meta data (of configurable width) for alignment with timestamps 32bit second and 32bit nanosecond time format for timestamps 32bit counter which counts any detected edge (can be used to detect missed edges) Timestamp buffer of configurable depth
Performance	Input signal max frequency depends partly on clock frequency but mainly on register access speed Burst handling via timestamp buffer
Portability	Vendor independent, written in plain VHDL Low footprint and low frequency requirements
Registers	Axi4 lite slave support for timestamp reading

Deliverables:

- Ip core in plain VHDL
- Testbench in plain VHDL
- Reference Design
  - Top level VHDL file
  - Timing Constraint SDC files
  - Vivado/Quartus Project file
- Linux Driver

Related Products:

- PTP Ordinary Clock
- PTP Grandmaster Clock
- PTP Hybrid Clock
- PPS Master/Slave
- IRIG Master/Slave
- Adjustable Clock
- Signal Generator

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