ClkDynamicControl

Reference Manual

Product Info	
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Overview

NetTimeLogic's Clock (CLK) Dynamic Control Core (DynamicControl) is a versatile solution designed for dynamic PI Servo adjustments in applications where ultra-high accuracy is essential. This documentation outlines the core capabilities, functions, and architecture, providing a comprehensive guide for integrating Dynamic Control into your system.

Key Features:

- Dynamic change of PI Servo Parameters via AXI4Lite
- 3 sets of PI Servo Parameters individually for Offset and Drift
- Individual adjustments of Drift and Offset
- Individual thresholds for Drift and Offset for when a set of PI Servo Parameters shall be applied (2 per Drift, 2 per Offset)
- Build time Configurable Sample Windows for Drift and Offset range checks
- Optional Logging of raw calculated Drift and Offset
- AXI4Lite register set or static configuration

Revision History

This table shows the revision history of this document.

Version	Date	Revision
0.1	16.04.2025	First draft

Table 1: Revision History

Content

Definitions

Definitions	
PI Servo	Proportional and Integral Servo Loop

Table 2: Definitions

Abbreviations

Abbreviations	
AXI	AMBA4 Specification (Stream and Memory Mapped)
PPB	Parts Per Billion
CLK	Clock
TB	Testbench
LUT	Look Up Table
FF	Flip Flop
RAM	Random Access Memory
ROM	Read Only Memory
FPGA	Field Programmable Gate Array
VHDL	Hardware description Language for FPGA's

Table 3: Abbreviations

1 Introduction

1.1 Context Overview

The Dynamic Control IP core plays a pivotal role in applications that demand ultra-precise frequency adjustments. Depending on raw calculated Offset and Drift values the PI Servo parameters on the Adjustable Counter Clock are adapted at runtime. The use-case behind the dynamic adaptation of PI Servo parameters is to allow for fast initial synchronization or resynchronization on a time jump. Parameters are adapted via AXI4 Lite Register access. The context block diagram (Figure 1) illustrates how Dynamic Control fits within the larger system.

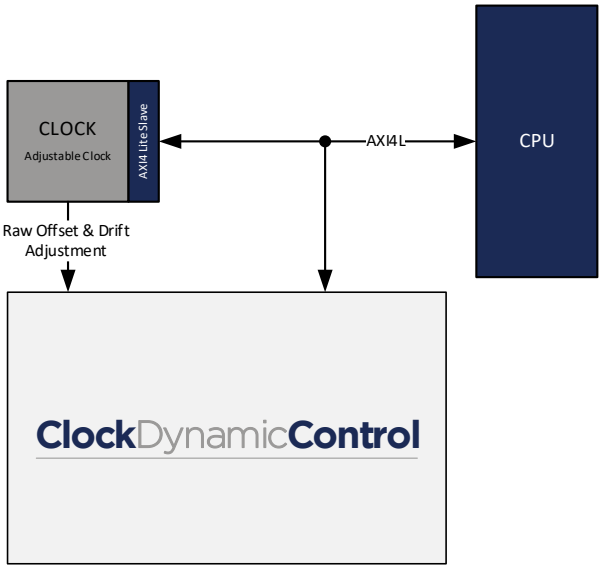

Figure 1: Context Block Diagram

1.2 Function

The Dynamic Control Core operates by receiving raw delta drift adjustments in delta parts per billion (delta PPB) as input and raw offset adjustments in nanoseconds. It then checks the adjustments if they are below a configurable threshold for a defined window and if all adjustments within the window are below the threshold, switches the PI Parameters to the Parameter Set associated with this threshold and writes the PI Parameters via AXI4 Lite to the Adjustable Counter Clock Core. There are individual thresholds for the PI Parameters Sets 1&2, Parameter Set 0 applies if the adjustments are not below any threshold. This applies individually for Offset and Drift.

2 Register Set

This is the register set of the Dynamic Control Module. It is accessible via AXI4Lite Memory Mapped. All registers are 32bit wide, no burst access, no unaligned access, no byte enables, no timeouts are supported. Register address space is not contiguous. Register addresses are only offsets in the memory area where the core is mapped in the AXI interconnects. Non existing register access in the mapped memory area is answered with a slave decoding error.

2.1 Register Overview

Registerset Overview			
Name	Description	Offset	Access
Clk DynamicControlControl Reg	Dynamic Control Enabled Control Register	0x00000000	RW
Clk DynamicControlStatus Reg	Dynamic Control Status Register	0x00000004	RO
Clk DynamicControlVersion Reg	Dynamic Control Version Register	0x0000000C	RO
Clk DynamicControlRawOffset Reg	Dynamic Control Raw Offset Register	0x00000010	RO
Clk DynamicControlRawDrift Reg	Dynamic Control Raw Drift Register	0x00000014	RO
Clk DynamicControlOffsetThresh1 Reg	Dynamic Control Offset Threshold for Parameters 1 Register	0x00000020	RW
Clk DynamicControlOffsetThresh2 Reg	Dynamic Control Offset Threshold for Parameters 2 Register	0x00000024	RW
Clk DynamicControlOffsetP0 Reg	Dynamic Control Offset Proportional Parameter 0 Register	0x00000028	RW
Clk DynamicControlOffsetI0 Reg	Dynamic Control Offset Integral Parameter 0 Register	0x0000002C	RW
Clk DynamicControlOffsetP1 Reg	Dynamic Control Offset Proportional Parameter 1 Register	0x00000030	RW
Clk DynamicControlOffsetI1 Reg	Dynamic Control Offset Integral Parameter 1 Register	0x00000034	RW
Clk DynamicControlOffsetP2 Reg	Dynamic Control Offset Proportional Parameter 2 Register	0x00000038	RW
Clk DynamicControlOffsetI2 Reg	Dynamic Control Offset Integral Parameter 2 Register	0x0000003C	RW
Clk DynamicControlDriftThresh1 Reg	Dynamic Control Drift Threshold for Parameters 1 Register	0x00000040	RW
Clk DynamicControlDriftThresh2 Reg	Dynamic Control Drift Threshold for Parameters 2 Register	0x00000044	RW

Clk DynamicControlDriftP0 Reg	Dynamic Control Drift Proportional Parameter 0 Register	0x00000048	RW
Clk DynamicControlDriftI0 Reg	Dynamic Control Drift Integral Parameter 0 Register	0x0000004C	RW
Clk DynamicControlDriftP1 Reg	Dynamic Control Drift Proportional Parameter 1 Register	0x00000050	RW
Clk DynamicControlDriftI1 Reg	Dynamic Control Drift Integral Parameter 1 Register	0x00000054	RW
Clk DynamicControlDriftP2 Reg	Dynamic Control Drift Proportional Parameter 2 Register	0x00000058	RW
Clk DynamicControlDriftI2 Reg	Dynamic Control Drift Integral Parameter 2 Register	0x0000005C	RW

2.2 Register Descriptions

2.2.1 General

2.2.1.1 CLK Dynamic Control Control Register

Used for general control over the Dynamic Control Module. Dynamic Offset and Drift can be enabled separately and there is a general enable.

Clk DynamicControlControl Reg																													
Reg Description																													
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RO																													DYN_DRIFT	DYN_OFFSET	ENABLE
RO																													RW	RW	RW
Reset: 0x00000000																															
Offset: 0x0000																															

Name	Description	Bits	Access
-	Reserved, read 0	Bit: 31:3	RO
DYN_DRIFT	Dynamic Drift PI Parameters Enable	Bit: 2	RW

DYN_OFFSET	Dynamic Offset PI Parameters Enable	Bit: 1	RW
ENABLE	Enable	Bit: 0	RW

2.2.1.2 CLK Dynamic Control Status Register

Shows which set of PI Parameters is selected.

Clk DynamicControlStatus Reg																													
Reg Description																													
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-																										DRIFT_PI_SEL		-		OFFSET_PI_SEL	
RO																										RO		RO		RO	
Reset: 0x00000000																															
Offset: 0x0004																															

Name	Description	Bits	Access
-	Reserved, read 0	Bit: 31:6	RO
DRIFT_PI_SEL	Which PI Parameter Set was selected for Drift, 0-2 (3 is unknown)	Bit: 5:4	RO
-	Reserved, read 0	Bit: 3:2	RO
OFFSET_PI_SEL	Which PI Parameter Set was selected for Offset, 0-2 (3 is unknown)	Bit: 1:0	RO

2.2.1.3 CLK Dynamic Control Version Register

Shows the version of the core.

Clk DynamicControlVersion Reg																															
Reg Description																															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VERSION																															
RO																															
Reset: 0xXXXXXXXX																															
Offset: 0x000C																															

Name	Description	Bits	Access
VERSION	Version of the IP core	Bit: 31:0	RO

2.2.1.4 CLK Dynamic Control Raw Offset Register

This is the raw offset before any filtering coming from the selected source.

Clk DynamicControlRawOffset Reg																															
Reg Description																															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OFFSET_SIGN	OFFSET_NS																														
RO	RO																														
Reset: 0x00000000																															
Offset: 0x0010																															

Name	Description	Bits	Access
OFFSET_SIGN	Sign bit: 0 = positive, 1 = negative	Bit: 31	RO
OFFSET_NS	Last calculated raw Offset value in Nanoseconds	Bit: 30:0	RO

2.2.1.5 CLK Dynamic Control Raw Drift Register

This is the raw drift before any filtering coming from the selected source.

Clk DynamicControlRawDrift Reg

Reg Description

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DRIFT_SIGN	DRIFT_NS																														
RO	RO																														

Reset: 0x00000000

Offset: 0x0014

Name	Description	Bits	Access
DRIFT_SIGN	Sign bit: 0 = positive, 1 = negative	Bit: 31	RO
DRIFT_NS	Last calculated raw Drift value in Nanoseconds/Second (ppb)	Bit: 30:0	RO

2.2.1.6 CLK Dynamic Control Offset Threshold 1 Register

This is the threshold to apply the Offset PI Parameter Set 1.

Clk DynamicControlOffsetThreshold1 Reg																															
Reg Description																															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OFFSET_TH_NS_1																															
RW																															
Reset: 0x000003E8																															
Offset: 0x0020																															

Name	Description	Bits	Access
OFFSET_TH_NS_1	Offset Threshold to apply Parameter set 1 (default 1000ns)	Bit: 31:0	RW

2.2.1.7 CLK Dynamic Control Offset Threshold 2 Register

This is the threshold to apply the Offset PI Parameter Set 2.

Clk DynamicControlOffsetThreshold2 Reg																															
Reg Description																															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OFFSET_TH_NS_2																															
RW																															
Reset: 0x00000064																															
Offset: 0x0024																															

Name	Description	Bits	Access
OFFSET_TH_NS_2	Offset Threshold to apply Parameter set 1 (default 100ns)	Bit: 31:0	RW

2.2.1.8 CLK Dynamic Control Offset Factor P 0 Register

This is the Proportional factor of the PI Servo Parameter Set 0.

Clk DynamicControlOffsetFactorP0 Reg																															
Reg Description																															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
																OFFSET_FACTOR_P0															
RO																RW															
Reset: 0x00004000																															
Offset: 0x0028																															

Name	Description	Bits	Access
-	Reserved, read 0	Bit: 31:16	RO
OFFSET_FACTOR_P0	Offset Proportional Factor as a fraction of 2^16, Set 0 (default 1/4)	Bit: 15:0	RW

2.2.1.9 CLK Dynamic Control Offset Factor I 0 Register

This is the Integral factor of the PI Servo Parameter Set 0.

Clk DynamicControlOffsetFactorI0 Reg																															
Reg Description																															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
																OFFSET_FACTOR_I0															
RO																RW															
Reset: 0x00000000																															
Offset: 0x002C																															

Name	Description	Bits	Access
-	Reserved, read 0	Bit: 31:16	RO
OFFSET_FACTOR_I0	Offset Integral Factor as a fraction of 2^16, Set 0 (default 0)	Bit: 15:0	RW

2.2.1.10 CLK Dynamic Control Offset Factor P 1 Register

This is the Proportional factor of the PI Servo Parameter Set 1.

Clk DynamicControlOffsetFactorP1 Reg																															
Reg Description																															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
																OFFSET_FACTOR_P1															
RO																RW															
Reset: 0x00001000																															
Offset: 0x0030																															

Name	Description	Bits	Access
-	Reserved, read 0	Bit: 31:16	RO
OFFSET_FACTOR_P1	Offset Proportional Factor as a fraction of 2^16, Set 1 (default 1/16)	Bit: 15:0	RW

2.2.1.11 CLK Dynamic Control Offset Factor I 1 Register

This is the Integral factor of the PI Servo Parameter Set 1.

Clk DynamicControlOffsetFactorI1 Reg																															
Reg Description																															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
																OFFSET_FACTOR_I1															
RO																RW															
Reset: 0x00000000																															
Offset: 0x0034																															

Name	Description	Bits	Access
-	Reserved, read 0	Bit: 31:16	RO
OFFSET_FACTOR_I1	Offset Integral Factor as a fraction of 2^16, Set 1 (default 0)	Bit: 15:0	RW

2.2.1.12 CLK Dynamic Control Offset Factor P 2 Register

This is the Proportional factor of the PI Servo Parameter Set 2.

Clk DynamicControlOffsetFactorP2 Reg																															
Reg Description																															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
																OFFSET_FACTOR_P2															
RO																RW															
Reset: 0x00000200																															
Offset: 0x0038																															

Name	Description	Bits	Access
-	Reserved, read 0	Bit: 31:16	RO
OFFSET_FACTOR_P2	Offset Proportional Factor as a fraction of 2^16, Set 2 (default 1/128)	Bit: 15:0	RW

2.2.1.13CLK Dynamic Control Offset Factor I 2 Register

This is the Integral factor of the PI Servo Parameter Set 2.

Clk DynamicControlOffsetFactorI2 Reg																															
Reg Description																															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
																OFFSET_FACTOR_I2															
RO																RW															
Reset: 0x00000000																															
Offset: 0x003C																															

Name	Description	Bits	Access
-	Reserved, read 0	Bit: 31:16	RO
OFFSET_FACTOR_I2	Offset Integral Factor as a fraction of 2^16, Set 2 (default 0)	Bit: 15:0	RW

2.2.1.14 CLK Dynamic Control Drift Threshold 1 Register

This is the threshold to apply the Drift PI Parameter Set 1.

Clk DynamicControlDriftThreshold1 Reg																															
Reg Description																															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DRIFT_TH_NS_1																															
RW																															
Reset: 0x00000064																															
Offset: 0x0040																															

Name	Description	Bits	Access
DRIFT_TH_NS_1	Drift Threshold to apply Parameter set 1 (default 100ns)	Bit: 31:0	RW

2.2.1.15CLK Dynamic Control Drift Threshold 2 Register

This is the threshold to apply the Drift PI Parameter Set 2.

Clk DynamicControlDriftThreshold2 Reg																															
Reg Description																															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DRIFT_TH_NS_2																															
RW																															
Reset: 0x00000020																															
Offset: 0x0044																															

Name	Description	Bits	Access
DRIFT_TH_NS_2	Drift Threshold to apply Parameter set 1 (default 20ns)	Bit: 31:0	RW

2.2.1.16CLK Dynamic Control Drift Factor P 0 Register

This is the Proportional factor of the PI Servo Parameter Set 0.

Clk DynamicControlDriftFactorP0 Reg																															
Reg Description																															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
																DRIFT_FACTOR_P0															
RO																RW															
Reset: 0x00001000																															
Offset: 0x0048																															

Name	Description	Bits	Access
-	Reserved, read 0	Bit: 31:16	RO
DRIFT_FACTOR_P0	Drift Proportional Factor as a fraction of 2^16, Set 0 (default 1/16)	Bit: 15:0	RW

2.2.1.17 CLK Dynamic Control Drift Factor I 0 Register

This is the Integral factor of the PI Servo Parameter Set 0.

Clk DynamicControlDriftFactorI0 Reg																															
Reg Description																															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
																DRIFT_FACTOR_I0															
RO																RW															
Reset: 0x00000000																															
Offset: 0x004C																															

Name	Description	Bits	Access
-	Reserved, read 0	Bit: 31:16	RO
DRIFT_FACTOR_I0	Drift Integral Factor as a fraction of 2^16, Set 0 (default 0)	Bit: 15:0	RW

2.2.1.18CLK Dynamic Control Drift Factor P 1 Register

This is the Proportional factor of the PI Servo Parameter Set 1.

Clk DynamicControlDriftFactorP1 Reg																															
Reg Description																															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
																DRIFT_FACTOR_P1															
RO																RW															
Reset: 0x00000800																															
Offset: 0x0050																															

Name	Description	Bits	Access
-	Reserved, read 0	Bit: 31:16	RO
DRIFT_FACTOR_P1	Drift Proportional Factor as a fraction of 2^16, Set 1 (default 1/32)	Bit: 15:0	RW

2.2.1.19CLK Dynamic Control Drift Factor I 1 Register

This is the Integral factor of the PI Servo Parameter Set 1.

Clk DynamicControlDriftFactorI1 Reg																															
Reg Description																															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
																DRIFT_FACTOR_I1															
RO																RW															
Reset: 0x00000000																															
Offset: 0x0054																															

Name	Description	Bits	Access
-	Reserved, read 0	Bit: 31:16	RO
DRIFT_FACTOR_I1	Drift Integral Factor as a fraction of 2^16, Set 1 (default 0)	Bit: 15:0	RW

2.2.1.20 CLK Dynamic Control Drift Factor P 2 Register

This is the Proportional factor of the PI Servo Parameter Set 2.

Clk DynamicControlDriftFactorP2 Reg																															
Reg Description																															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
																DRIFT_FACTOR_P2															
RO																RW															
Reset: 0x00000080																															
Offset: 0x0058																															

Name	Description	Bits	Access
-	Reserved, read 0	Bit: 31:16	RO
DRIFT_FACTOR_P2	Drift Proportional Factor as a fraction of 2^16, Set 2 (default 1/512)	Bit: 15:0	RW

2.2.1.21CLK Dynamic Control Drift Factor I 2 Register

This is the Integral factor of the PI Servo Parameter Set 2.

Clk DynamicControlDriftFactorI2 Reg																															
Reg Description																															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
																DRIFT_FACTOR_I2															
RO																RW															
Reset: 0x00000000																															
Offset: 0x005C																															

Name	Description	Bits	Access
-	Reserved, read 0	Bit: 31:16	RO
DRIFT_FACTOR_I2	Drift Integral Factor as a fraction of 2^16, Set 2 (default 0)	Bit: 15:0	RW

3 Design Description

3.1 Top Level – CLK Dynamic Control

3.1.1.1 Parameters

The core must be parametrized at synthesis time. There are a couple of parameters which define the final behavior and resource usage of the core.

Name	Type	Size	Description
StaticConfig_Gen	boolean	1	If Static Configuration or AXI is used: true = Static, false = AXI
ClockClkPeriodNano-second_Gen	natural	1	Clock Period in Nanosecond: Default for 50 MHz = 20 ns, if non-integer only the nanosec-onds part here
OffsetRangeSample Window_Gen	natural	1	Window of how many Offset samples must be below a threshold to switch parame-ters
DriftRangeSample Window_Gen	natural	1	Window of how many Drift samples must be below a threshold to switch parame-ters
AxiTimeout Nanosecond_Gen	natural	1	0 means no timeout (wait forever)
ClockAxiAddress RangeLow_Gen	std_logic_vector	32	AXI Base Address of the Adjustable Counter Clock IP
ClockAxiAddress RangeHigh_Gen	std_logic_vector	32	AXI Base Address plus Regis-terset Size of the Adjustable Counter Clock IP Default plus 0xFFFF
LogRaw Adjustments_Gen	boolean	1	Log the Raw Adjustments
AxiAddressRange Low_Gen	std_logic_vector	32	AXI Base Address

AxiAddressRange High_Gen	std_logic_vector	32	AXI Base Address plus Register-set Size Default plus 0xFFFF
Sim_Gen	boolean	1	If in Testbench simulation mode: true = Simulation, false = Synthesis

Table 4: Parameters

3.1.1.2 Structured Types

3.1.1.2.1 Clk_Time_Type

Defined in Clk_Package.vhd of library ClkLib
Type represents the time used everywhere. For this type overloaded operators + and – with different parameters exist.

Field Name	Type	Size	Description
Second	std_logic_vector	32	Seconds of time
Nanosecond	std_logic_vector	32	Nanoseconds of time
Fraction	std_logic_vector	2	Fraction numerator (mostly not used)
Sign	std_logic	1	Positive or negative time, 1 = negative, 0 = positive.
TimeJump	std_logic	1	Marks when the clock makes a time jump (mostly not used)

Table 5: Clk_Time_Type

3.1.1.2.2 Clk_TimeAdjustment_Type

Defined in Clk_Package.vhd of library ClkLib
Type represents the time used everywhere. For this type overloaded operators + and – with different parameters exist.

Field Name	Type	Size	Description
TimeAdjustment	Clk_Time_Type	1	Time to adjust
Interval	std_logic_vector	32	Adjustment interval, for the

			drift correction this is the denumerator of the rate in nanoseconds (TimeAdjustment every Interval = drift rate), for offset correction this is the period in which the time shall be corrected (TimeAdjustment in Interval), for setting the time, this has no mining.
Valid	std_logic	1	If the Adjustment is valid

Table 6: Clk_TimeAdjustment_Type

3.1.1.2.3 Clk_CoreInfo_Type

Defined in Clk_Package.vhd of library ClkLib
This is the type used for getting info about the cores state status.

Field Name	Type	Size	Description
State	Clk_CoreState_Type	1	State of the core: Unknown_E, Slave_E or Master_E
Accuracy	std_logic_vector	8	Accuracy of the core, higher is better
Enabled	std_logic	1	If the core is enabled
InSync	std_logic	1	If the core is synchronized
Error	std_logic	1	If the core has an error

Table 7: Clk_CoreInfo_Type

3.1.1.2.4 Clk_UtcInfo_Type

Defined in Clk_Package.vhd of library ClkLib
This is the type used for getting info about the UTC status.

Field Name	Type	Size	Description
UtcOffset	std_logic_vector	16	UTC Offset to TAI
UtcOffsetValid	std_logic	1	If UTC Info is valid
Leap59	std_logic	1	Leap 59 event

Leap61	std_logic	1	Leap 61 event

Table 8: Clk_UtcInfo_Type

3.1.1.2.5 Clk_ClockStaticStatus_Type

Defined in Clk_ClockAddrPackage.vhd of library ClkLib
This is the type used for static status.

Field Name	Type	Size	Description
CoreInfo	Clk_CoreInfo_ Type	1	Info about the Cores state
UtcInfo	Clk_UtcInfo_ Type	1	Info about the UTC state
OffsetAdjustmentRaw	Clk_TimeAdjust ment_Type	1	Offset Adjustment Raw
OffsetAdjustment	Clk_TimeAdjust ment_Type	1	Offset Adjustment
OffsetAdjustment Fract	std_logic_vector	16	Fraction Offset Adjustments
DriftAdjustmentRaw	Clk_TimeAdjust ment_Type	1	Drift Adjustment Raw
DriftAdjustment	Clk_TimeAdjust ment_Type	1	Drift Adjustment
DriftAdjustment Fract	std_logic_vector	16	Fraction Drift Adjustments
DriftCountAdjustment	Clk_DriftCountA djustment_Type	1	Drift single Adjustments
ClockTime	Clk_Time_Type	1	Time of the Clock
ClockSelect	std_logic_vector	16	Clock Selection

Table 9: Clk_ClockStaticStatus_Type

3.1.1.2.6 Clk_ClockStaticStatusVal_Type

Defined in Clk_ClockAddrPackage.vhd of library ClkLib
This is the type used for valid flags of the static status.

Field Name	Type	Size	Description

CoreInfo_Val	std_logic	1	Core Info is valid
UtcInfo_Val	std_logic	1	UTC Info is valid
OffsetAdjustment_Val	std_logic	1	Offset Adjustment valid
DriftAdjustment_Val	std_logic	1	Drift Adjustment valid
OffsetAdjustment Raw_Val	std_logic	1	Offset Adjustment valid
DriftAdjustment Raw_Val	std_logic	1	Drift Adjustment valid
ClockTime_Val	std_logic	1	Time is valid

Table 10: Clk_ClockStaticStatusVal_Type

3.1.1.2.7 Clk_DynamicControlStaticConfig_Type

Defined in Clk_DynamicControlAddrPackage.vhd of library ClkLib
This is the type used for static configuration.

Field Name	Type	Size	Description
OffsetThreshold1	std_logic_vector	32	Offset Threshold for Parameter set 1
OffsetThreshold2	std_logic_vector	32	Offset Threshold for Parameter set 2
OffsetFactorP0	std_logic_vector	16	Offset PI Proportional Parameter 0
OffsetFactorI0	std_logic_vector	16	Offset PI Integral Parameter 0
OffsetFactorP1	std_logic_vector	16	Offset PI Proportional Parameter 1
OffsetFactorI1	std_logic_vector	16	Offset PI Integral Parameter 1
OffsetFactorP2	std_logic_vector	16	Offset PI Proportional Parameter 2
OffsetFactorI2	std_logic_vector	16	Offset PI Integral Parameter 2
DriftThreshold1	std_logic_vector	32	Drift Threshold for Parameter set 1
DriftThreshold2	std_logic_vector	32	Drift Threshold for Parameter set 2
DriftFactorP0	std_logic_vector	16	Drift PI Proportional Parameter 0
DriftFactorI0	std_logic_vector	16	Drift PI Integral Parameter 0

DriftFactorP1	std_logic_vector	16	Drift PI Proportional Parameter 1
DriftFactorI1	std_logic_vector	16	Drift PI Integral Parameter 1
DriftFactorP2	std_logic_vector	16	Drift PI Proportional Parameter 2
DriftFactorI2	std_logic_vector	16	Drift PI Integral Parameter 2

Table 11: Clk_DynamicControlStaticConfig_Type

3.1.1.2.8 Clk_DynamicControlStaticConfigVal_Type

Defined in Clk_DynamicControlAddrPackage.vhd of library ClkLib
This is the type used for valid flags of the static configuration.

Field Name	Type	Size	Description
Enable_Val	std_logic	1	Enables the Dynamic Control
DynamicOffset Factor_Val	std_logic	1	Enables Dynamic Offset Factor applying
DynamicDrift Factor_Val	std_logic	1	Enables Dynamic Drift Factor applying

Table 12: Clk_DynamicControlStaticConfigVal_Type

3.1.1.2.9 Clk_DynamicControlStaticStatus_Type

Defined in Clk_ DynamicControlAddrPackage of library ClkLib
This is the type used for static status.

Field Name	Type	Size	Description
CoreInfo	Clk_CoreInfo_ Type	1	Info about the Cores state
UtcInfo	Clk_UtcInfo_ Type	1	Info about the UTC state
RangeOffsetSelected	std_logic_vector	2	Offset Range Selected
RangeDriftSelected	std_logic_vector	2	Drift Range Selected

Table 13: Clk_DynamicControlStaticStatus_Type

3.1.1.2.10 Clk_DynamicControlStaticStatusVal_Type

Defined in Clk_DynamicControlAddrPackage.vhd of library ClkLib
This is the type used for valid flags of the static status.

Field Name	Type	Size	Description
CoreInfo_Val	std_logic	1	Core Info is valid
UtcInfo_Val	std_logic	1	UTC Info is valid

Table 14: Clk_DynamicControlStaticStatusVal_Type

3.1.1.3 Entity Block Diagram

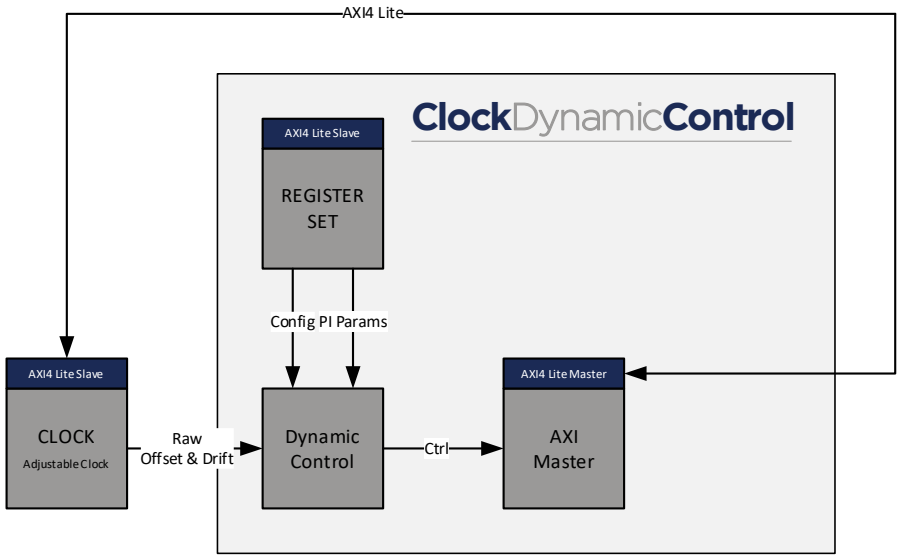

Figure 2: Dynamic Control Block Diagram

3.1.1.4 Entity Description

At the highest level, the Dynamic Control IP core manages the entire process of dynamic PI Servo Parameter adjusting. It receives the raw offset and drift adjustments from the Adjustable Counter Clock IP and decides based these values and thresholds which PI Servo Parameter set shall be applied to the Adjustable Counter Clock IP and written via AXI4 Lite. Thresholds and PI Parameters can be configured via AXI4 Lite.

3.1.1.5 Entity Declaration

Name	Dir	Type	Size	Description
Generics				

General				
StaticConfig_Gen	-	boolean	1	If Static Configuration or AXI is used: true = Static, false = AXI
ClockClkPeriodNanosecond_Gen	-	natural	1	Clock Period in Nanosecond: Default for 50 MHz = 20 ns, if non-integer only the nanoseconds part here
OffsetRangeSampleWindow_Gen	-	natural	1	Window of how many Offset samples must be below a threshold to switch parameters
DriftRangeSampleWindow_Gen	-	natural	1	Window of how many Drift samples must be below a threshold to switch parameters
AxiTimeoutNanosecond_Gen	-	natural	1	0 means no timeout (wait forever)
ClockAxiAddressRangeLow_Gen	-	std_logic_vector	32	AXI Base Address of the Adjustable Counter Clock IP
ClockAxiAddressRangeHigh_Gen	-	std_logic_vector	32	AXI Base Address plus Registerset Size of the Adjustable Counter Clock IP Default plus 0xFFFF
LogRawAdjustments_Gen	-	boolean	1	Log the Raw Adjustments
AxiAddressRangeLow_Gen	-	std_logic_vector	32	AXI Base Address
AxiAddressRangeHigh_Gen	-	std_logic_vector	32	AXI Base Address plus Registerset

				Size Default plus 0xFFFF
Sim_Gen	-	boolean	1	If in Testbench simulation mode: true = Simulation, false = Synthesis
System				
SysClk_ClkIn	in	std_logic	1	System Clock
SysRstN_RstIn	in	std_logic	1	System Reset
Clock Status				
ClkStaticSta-tusClock_DatIn	in	Clk_ClockStatic Status_Type	1	Clock Static Status (holds drift adjust-ment)
ClkStaticSta-tusClock_ValIn	in	Clk_ClockStatic StatusVal_Type	1	Clock Static Status valid
Static Config				
StaticConfig_DatIn	in	Clk_DynamicControl StaticConfig_Type	1	Static Config
StaticConfig_ValIn	in	Clk_DynamicControl StaticConfig Val_Type	1	Static Config valid
Static Status				
StaticStatus_DatOut	out	Clk_DynamicControl StaticStatus_Type	1	Static Status
StaticStatus_ValOut	out	Clk_DynamicControl StaticStatusVal_Type	1	Static Status valid
AXI4 Lite Slave				
AxiWriteAddrValid _ValIn	in	std_logic	1	Write Address Valid
AxiWriteAddrReady _RdyOut	out	std_logic	1	Write Address Ready
AxiWriteAddrAddress _AdrIn	in	std_logic_vector	32	Write Address
AxiWriteAddrProt _DatIn	in	std_logic_vector	3	Write Address Protocol
AxiWriteDataValid _ValIn	in	std_logic	1	Write Data Valid
AxiWriteDataReady _RdyOut	out	std_logic	1	Write Data Ready
AxiWriteDataData _DatIn	in	std_logic_vector	32	Write Data
AxiWriteDataStrobe _DatIn	in	std_logic_vector	4	Write Data Strobe

AxiWriteRespValid_ValOut	out	std_logic	1	Write Response Valid
AxiWriteRespReady_RdyIn	in	std_logic	1	Write Response Ready
AxiWriteResp Response_DatOut	out	std_logic_vector	2	Write Response
AxiReadAddrValid_ValIn	in	std_logic	1	Read Address Valid
AxiReadAddrReady_RdyOut	out	std_logic	1	Read Address Ready
AxiReadAddrAddress_AdrIn	in	std_logic_vector	32	Read Address
AxiReadAddrProt_DatIn	in	std_logic_vector	3	Read Address Protocol
AxiReadDataValid_ValOut	out	std_logic	1	Read Data Valid
AxiReadDataReady_RdyIn	in	std_logic	1	Read Data Ready
AxiReadData Response_DatOut	out	std_logic_vector	2	Read Data
AxiReadDataData_DatOut	out	std_logic_vector	32	Read Data Re-sponse
AxiWriteAddr Valid_ValOut	out	std_logic	1	Write Address Valid
AxiWriteAddr Ready_RdyIn	in	std_logic	1	Write Address Ready
AxiWriteAddr Address_AdrOut	out	std_logic_vector	32	Write Address
AxiWriteAddr Prot_DatOut	out	std_logic_vector	3	Write Address Protocol
AxiWriteData Valid_ValOut	out	std_logic	1	Write Data Valid
AxiWriteData Ready_RdyIn	in	std_logic	1	Write Data Ready
AxiWriteData Data_DatOut	out	std_logic_vector	32	Write Data
AxiWriteData Strobe_DatOut	out	std_logic_vector	4	Write Data Strobe
AxiWriteResp Valid_ValIn	in	std_logic	1	Write Response Valid
AxiWriteResp Ready_RdyOut	out	std_logic	1	Write Response Ready
AxiWriteResp Response_DatIn	in	std_logic_vector	2	Write Response
AxiReadAddr Valid_ValOut	out	std_logic	1	Read Address Valid

AxiReadAddr Ready_RdyIn	in	std_logic	1	Read Address Ready
AxiReadAddr Address_AdrOut	out	std_logic_vector	32	Read Address
AxiReadAddr Prot_DatOut	out	std_logic_vector	3	Read Address Protocol
AxiReadData Valid_ValIn	in	std_logic	1	Read Data Valid
AxiReadData Ready_RdyOut	out	std_logic	1	Read Data Ready
AxiReadData Response_DatIn	in	std_logic_vector	2	Read Data Response
AxiReadData Data_DatIn	in	std_logic_vector	32	Read Data

Table 15: Dynamic Control Entity Declaration

3.2 Configuration example

In both cases the enabling of the core shall be done last, after or together with the configuration.

3.2.1 Static Configuration

```
constant ClkStaticConfig_Con : Clk_ClockStaticConfig_Type := (
  OffsetThreshold1               => x"000003E8",
  OffsetThreshold2               => x"00000064",
  OffsetFactorP0                 => x"4000",
  OffsetFactorI0                 => x"0000",
  OffsetFactorP1                 => x"1000",
  OffsetFactorI1                 => x"0000",
  OffsetFactorP2                 => x"0200",
  OffsetFactorI2                 => x"0000",
  DriftThreshold1                => x"00000064",
  DriftThreshold2                => x"00000014",
  DriftFactorP0                  => x"1000",
  DriftFactorI0                  => x"0000",
  DriftFactorP1                  => x"0800",
  DriftFactorI1                  => x"0000",
  DriftFactorP2                  => x"0080",
  DriftFactorI2                  => x"0000"
);

constant ClkStaticConfigVal_Con : Clk_ClockStaticConfigVal_Type := (
  Enable_Val                     => '1',
  DynamicOffsetFactor_Val        => '0',
  DynamicDriftFactor_Val         => '0'
);
```

Figure 3: Static Configuration

The PI Parameters should be set before enabling.

3.2.2 AXI Configuration

The following code is a simplified pseudocode from the testbench: The base address of the Clock is 0x10000000.

```
-- DYNAMIC CONTROL
-- Config
-- Offset 0: 1/4 P + 0 I
AXI AXI0 WRITE 10000028 00004000
AXI AXI0 WRITE 1000002C 00000000
-- Drift 0: 1/16 P + 0 I
AXI AXI0 WRITE 10000048 00001000
AXI AXI0 WRITE 1000004C 00000000
```

```
-- Offset 1: 1/16 P + 0 I
AXI AXI0 WRITE 10000030 00001000
AXI AXI0 WRITE 10000034 00000000
-- Drift 1: 1/32 P + 0 I
AXI AXI0 WRITE 10000050 00000800
AXI AXI0 WRITE 10000054 00000000
-- Offset Threshold 1: 1000
AXI AXI0 WRITE 10000020 000003E8
-- Drift Threshold 1: 100
AXI AXI0 WRITE 10000040 00000064

-- Offset 1: 1/128 P + 0 I
AXI AXI0 WRITE 10000038 00000200
AXI AXI0 WRITE 1000003C 00000000
-- Drift 1: 1/512 P + 0 I
AXI AXI0 WRITE 10000058 00000080
AXI AXI0 WRITE 1000005C 00000000
-- Offset Threshold 1: 100
AXI AXI0 WRITE 10000024 00000064
-- Drift Threshold 1: 20
AXI AXI0 WRITE 10000044 00000014

-- Enable, dynamic Offset and Drift PI Params
AXI AXI0 WRITE 10000000 00000007
```

Figure 4: AXI Configuration

The PI Servo Parameters and Threshold shall be set before enabling the Clock or dynamic adjustments.

3.3 Clocking and Reset Concept

3.3.1 Clocking

To keep the design as robust and simple as possible, the whole Dynamic Control and all other cores from NetTimeLogic are run in one clock domain. This is considered to be the system clock. Per Default this clock is 50MHz. Where possible also the interfaces are run synchronous to this clock. Clock domain crossings for the AXI interface is moved from the AXI slave to the AXI interconnect.

Clock	Frequency	Description
System		
System Clock	50MHz (Default)	System clock where the OC runs on as well as the counter clock etc.
AXI Interface		
AXI Clock	50MHz (Default)	Internal AXI bus clock, same as the system clock

Table 16: Clocks

3.3.2 Reset

In connection with the clocks, there is a reset signal for each clock domain. All resets are active low. All resets can be asynchronously set and shall be synchronously released with the corresponding clock domain. All resets shall be asserted for the first couple (around 8) clock cycles. All resets shall be set simultaneously and released simultaneously.

Reset	Polarity	Description
System		
System Reset	Active low	Asynchronous set, synchronous release with the system clock
AXI Interface		
AXI Reset	Active low	Asynchronous set, synchronous release with the AXI clock, which is the same as the system clock

Table 17: Resets

A List of tables

B List of figures