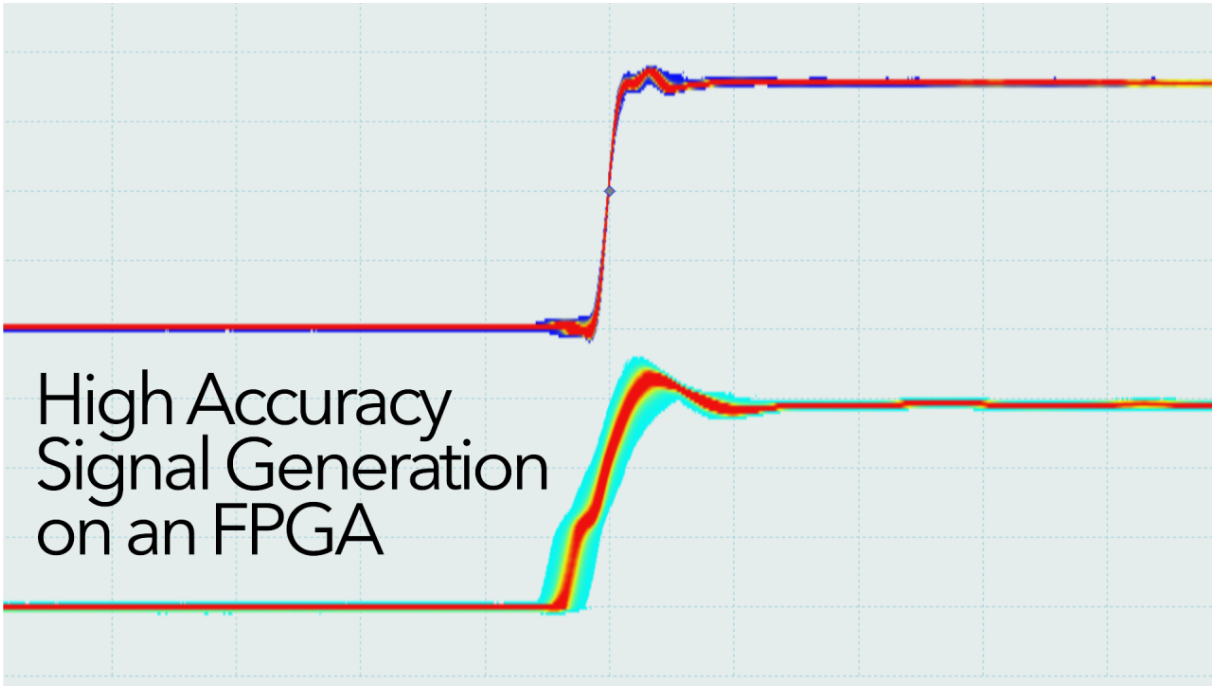

1 Nanosecond Signal Generation Accuracy on an FPGA

17. April 2024

Last week we talked about how to achieve a 1 Nanosecond Timestamp Accuracy on an FPGA using the Time-to-Digital Converter (TDC) mechanism: Read the article here

Today we describe how you can generate a signal with 1 Nanosecond (or better) Accuracy on an FPGA. As you might guess we again do not use a 1GHz clock to do this since as with the Timestamping this is not feasible on a low-cost FPGA.

The mechanism used to achieve this, is the opposite to TDC and is called **Digital-to-Time Converter (DTC)**. Again it is based on the **Tapped Delay Line (TDL)** scheme with **Carry Elements**. For a DTC with Carry Elements there are two possible schemes:

a) Load the chain at different positions with 0s and 1s and use the last Tap as the output

b) Use different Taps of the chain as the output and load the first chain element with 0 to 1 or 1 to 0 transitions.

For the first prototype we choose the scheme b) since it was the easier to do. In a later stage we will also look at the scheme a). The drawback of the b) scheme is that the multiplexing of the different Taps of the delay line requires LUTs which are connected via the normal routing resources and must be manually placed to achieve an as similar as possible delay of all Taps to the output signal. This is achievable if your goal is a 1ns resolution, for better resolutions the scheme a) might be more suitable.

We again use a 250MHz clock for feeding the chain (Carry Init) and the fine alignment to time and a 50MHz aligned clock for the coarse alignment to time. The chain has 3 Taps: one after each nanosecond of propagation delay. Depending on the desired delay one of the 3 Taps is feeding the output. 0&4 = 0ns after clock edge, 1 = 1ns after clock edge …

To have not only a 1ns resolution the output and internal delay of the signal (e.g. clock delay, FF to Carry Init, Carry Tap to LUT and LUT to ouput, etc.) needs to be compensated for.

There you have your Signal Generation with 1 ns accuracy!

Future Work

There are multiple papers about different schemes for building DTCs on FPGAs and we will see if we find a more suitable (easier to place, less possible inaccuracy sources) DTC scheme and implement it accordingly. On the rest of the signal generation this has no influence since we designed the DTC as an add-on to our signal generation modules which will otherwise just have a 4ns resolution.

Where do we use it?

The prototype DTC is now incorporated into the following NetTimeLogic IP cores:

- Signal Generator
- Frequency Generator
- PPS Master

The PPS Master is also integrated into our PPS Analyzer Solution which therefore now also supports 1 ns of accuracy on the PPS Output for cascading multiple PPS Analyzers.